Energy Metering Chipset for Polyphase Shunt Meters

Preliminary Technical Data

ADE7978/ADE7933/ADE7932

FEATURES

Enables shunt current sensors in polyphase energy meters
Immune to magnetic tampering
Highly accurate; supports EN 50470-1, EN 50470-3, IEC 62053-21, IEC 62053-22, IEC 62053-23, ANSI C12.20 and IEEE1459 standards
Compatible with 3-phase, 3- or 4-wire (delta or wye), and other 3-phase services
Computes active, reactive, and apparent energy, on each phase and on the overall system
Less than 0.25% error in active and reactive energy over a dynamic range of 2000 to 1 at T_A = 25°C
Less than 0.1% error in voltage and current rms over a dynamic range of 1000 to 1 at T_A = 25°C
Power quality measurements including THD
Wide-supply voltage operation: 2.4 V to 3.7 V
Reference: 1.2 V (drift 10 ppm/°C typical)
Single 3.3 V supply
Safety and regulatory approvals
UL recognition
5000 Vrms for 1 minute per UL 1577
CSA Components Acceptance Notice #5A
IEC 61010-1: 400V rms (basic)
VDE Certificate of Conformity
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
V_{IORM} = 846 V peak
Operating temperature: –40°C to +85°C
Flexible I²C, SPI, and HSDC serial interfaces

APPLICATIONS

Energy metering systems
Power monitoring

GENERAL DESCRIPTION

The ADE7978 and ADE7933/ADE7932 form a chipset dedicated to measuring 3-phase electrical energy measurement using shunts as current sensors.

The ADE7933/ADE7932 is an isolated three-input channel, analog to digital converter (ADC) for polyphase energy metering applications using shunt current sensors. It features three 24-bit analog to digital converters, each of which provides 70dB signal to noise ratio over a 3 kHz signal bandwidth. One channel is dedicated to measuring the voltage across a shunt when the shunt is used for current sensing. Two additional channels are dedicated to measuring voltages, which are usually sensed using resistor dividers. The ADE7933 and ADE7932 also measure the temperature of the IC. The ADE7932 is the same as the ADE7933 but it does not include the second voltage measurement.

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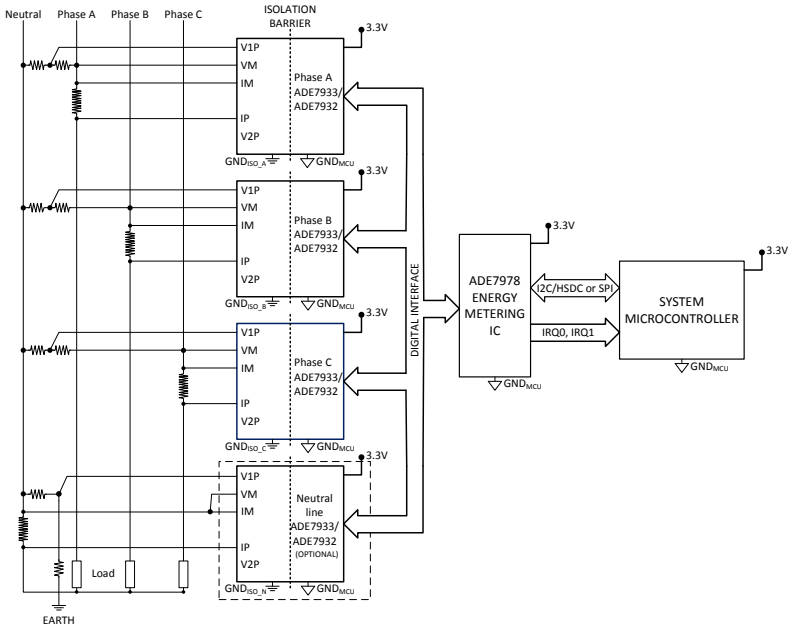

Figure 1. 3 Phase 4 Wire Meter with Four ADE7933/ADE7932s and One ADE7978

Rev. PrD

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The ADE7933/ADE7932 integrate an isolated dc-to-dc converter. Based on the Analog Devices, Inc., *iso*Power® technology, the dc-to-dc converter provides the regulated power required by the first stage of the ADCs. This device eliminates the need for an external dc-to-dc isolation block.

The *i*Coupler chip scale transformer technology is used to isolate the logic signals between the first and second stages of the ADC. The result is a small form factor, total isolation solution.

The ADE7933/ADE7932 contains a digital interface, specially designed to provide the ADE7978 access to its ADC outputs and other configuration settings.

The ADE7933/ADE7932 is available in the 20-lead wide body SOIC, Pb-free package with increased creepage.

The ADE7978 is a high accuracy, 3-phase electrical energy measurement IC with serial interfaces and three flexible pulse outputs. The ADE7978 may interface with up to four ADE7933/ADE7932s. It incorporates all the signal processing required to perform total (fundamental and harmonic) active, reactive and apparent energy measurement and rms calculations, as well as fundamental-only active and reactive energy measurement and rms calculations. A fixed function digital signal processor (DSP) executes this signal processing.

The ADE7978 measures the active, reactive, and apparent energy in various 3-phase configurations, such as wye or delta services, with both three and four wires. The ADE7978 provides system calibration features for each phase, gain calibration and optional offset correction. Phase compensation, although available, is not necessary because the currents are sensed using shunts. The CF1, CF2, and CF3 logic outputs provide a wide choice of power information: total active, reactive, and apparent powers, or the sum of the current rms values, and fundamental active and reactive powers.

The ADE7978 incorporates power quality measurements, such as short duration low or high voltage detections, short duration high current variations, line voltage period measurement, and angles between phase voltages and currents. Two serial interfaces, SPI and I^2C, can be used to communicate with the ADE7978. A dedicated high speed interface, the high speed data capture (HSDC) port, can be used in conjunction with I^2C to provide access to the ADC outputs and real-time power information. The ADE7978 also has two interrupt request pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$, to indicate that an enabled interrupt event has occurred. The ADE7978 is available in the 28-lead LFCSP, Pb-free package.

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FUNCTIONAL BLOCK DIAGRAMS

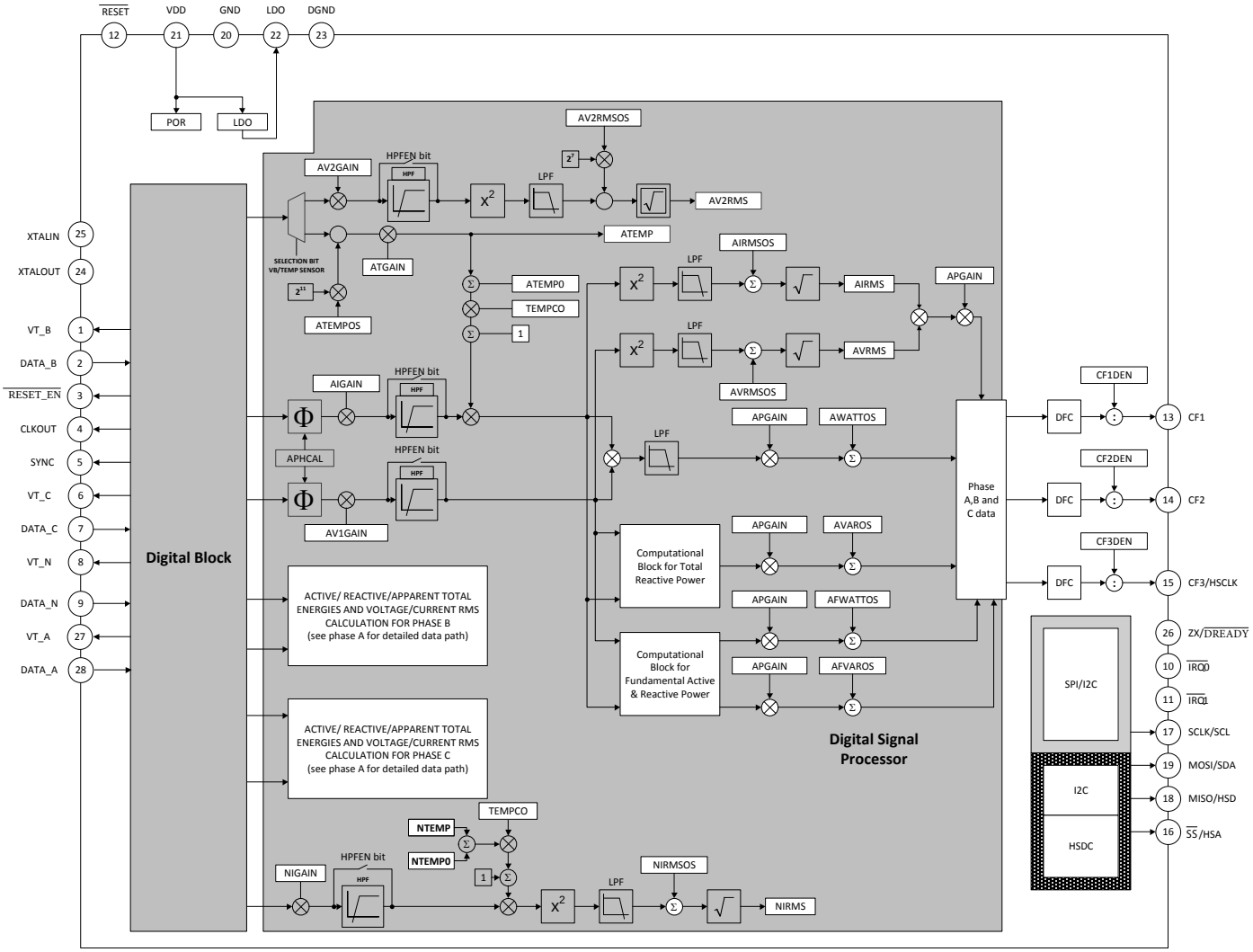


Figure 2. ADE7978 Functional Block Diagram

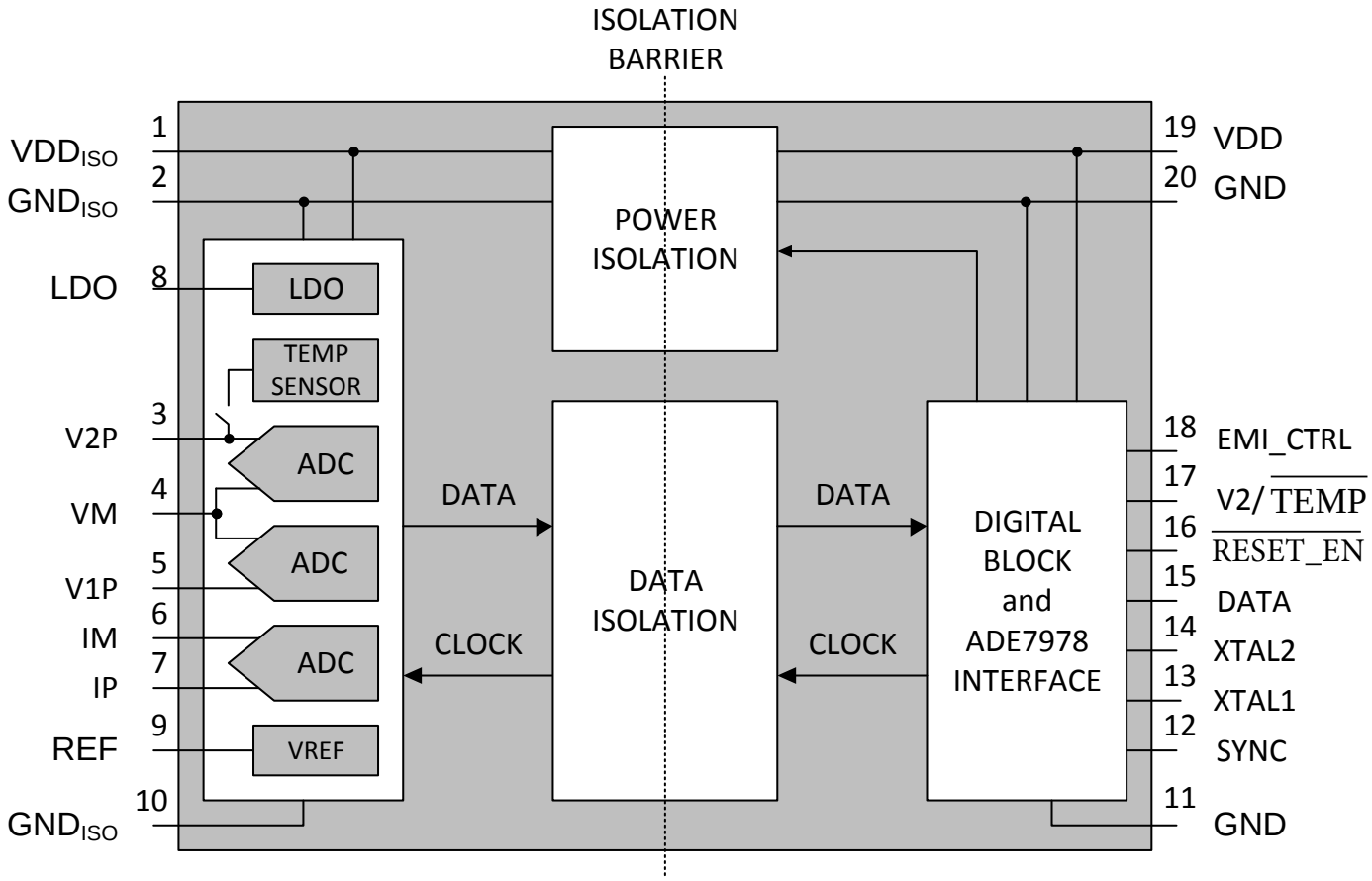


Figure 3. ADE7933 Functional Block Diagram

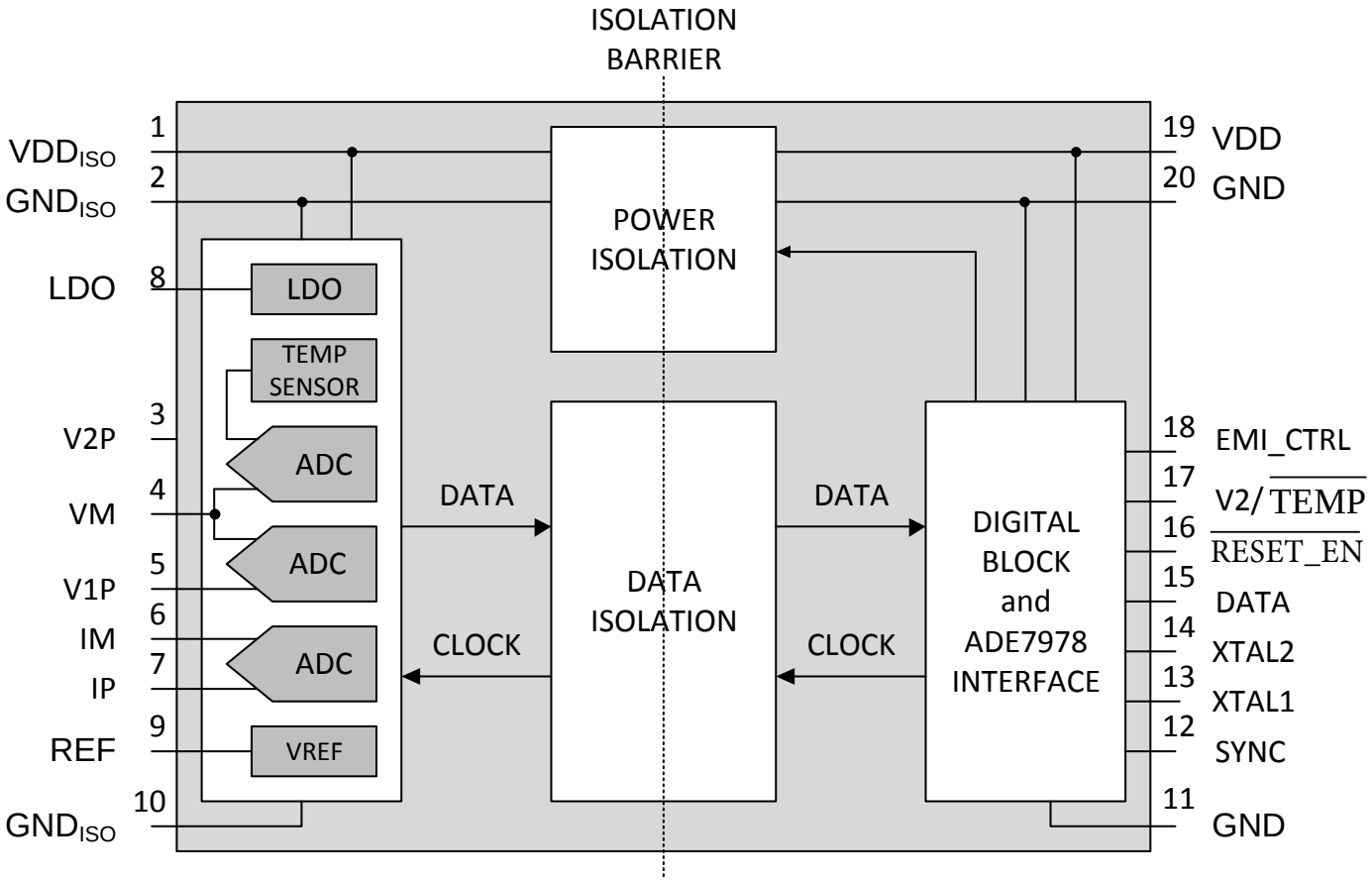


Figure 4. ADE7932 Functional Block Diagram

ADE7978 AND ADE7933/ADE7932 SYSTEM SPECIFICATIONS

VDD = 3.3 V ± 10%, GND = DGND = 0 V, XTALIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_{TYP}= 25°C.

Table 1.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY					
Active Energy Measurement					
Active Energy Measurement Error (per Phase)					
Total Active Energy		0.1		%	Over a dynamic range of 500 to 1, pf=1, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, pf=1
Fundamental Active Power		0.1		%	Over a dynamic range of 500 to 1, pf=1, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, pf=1
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz, IP= V1P= V2P= ±100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc
Output Frequency Variation		0.01		%	
Total Active Energy Measurement Bandwidth		3.3		kHz	
REACTIVE ENERGY MEASUREMENT					
Reactive Energy Measurement Error (per Phase)					
Total Reactive Power		0.1		%	Over a dynamic range of 500 to 1, pf=0, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, pf=0
Fundamental Reactive Power		0.1		%	Over a dynamic range of 500 to 1, pf=0, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, pf=0
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz, IP=V1P= V2P= ±100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc
Output Frequency Variation		0.01		%	
Total Reactive Energy Measurement Bandwidth		3.3		kHz	
RMS MEASUREMENTS					
I rms and V rms Measurement Bandwidth		3.3		kHz	
I rms and V rms Measurement Error		0.1		%	Over a dynamic range of 1000 to 1
WAVEFORM SAMPLING					Sampling CLKIN/2048, 16.384 MHz/2048 = 8 kSPS
Current and Voltage Channels					See the Waveform Sampling Mode section
Signal-to-Noise Ratio, SNR		70		dB	
Signal-to-Noise-and-Distortion Ratio, SINAD		60		dB	
Bandwidth (−3 dB)		3.3		kHz	
TIME INTERVAL BETWEEN PHASES					
Measurement Error		0.3		Degrees	Line frequency = 45 Hz to 65 Hz, HPF on
CF1, CF2, CF3 PULSE OUTPUTS					
Maximum Output Frequency		68.818		kHz	WTHR = VARTHR = VATHR = 3
Duty Cycle		50		%	If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1
		(1 + 1/CFDEN) × 50%			If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
Active Low Pulse Width		80		ms	If CF1, CF2, or CF3 frequency < 6.25 Hz
Jitter		0.04		%	For CF1, CF2, or CF3 frequency = 1 Hz and nominal phase currents are larger than 10% of full scale

[1] See the Typical Performance Characteristics section.
[2] See the Terminology section for a definition of the parameters.

ADE7978 SPECIFICATIONS

VDD = 3.3 V ± 10%, GND = DGND = 0 V, XTALIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_{TYP}= 25°C.

Table 2.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUT					All specifications CLKIN of 16.384 MHz
Input Clock Frequency CLKIN	16.22	16.384	16.55	MHz	
XTALIN logic inputs					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	
Crystal Equivalent Series Resistance	30		150	Ω	
XTALIN Input Capacitance[3]		20	30	pF	
XTALOUT Output Capacitance[3]		20	30	pF	
CLOCK OUTPUT					
Output Clock Frequency at CLKOUT pin		4.096		MHz	
Duty Cycle		50		%	
CLKOUT logic outputs					
Output High Voltage, V_{OH}	2.97			V	
Output Low Voltage, V_{OL}			0.4	V	
LOGIC INPUTS—MOSI/SDA, SCLK/SCL, $\overline{SS}$, DATA_A, DATA_B, DATA_C, DATA_N, $\overline{RESET\_EN}$					
Input High Voltage, V_{INH}	2.4			V	VDD = 3.3 V ± 10%
Input Current, I_{IN}		5	TBD	nA	Input=VDD=3.3V
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V ± 10%
Input Current, I_{IN}		40	TBD	nA	Input = 0 V, VDD = 3.3 V
Input Capacitance, C_{IN}			10	pF	
LOGIC INPUT— $\overline{RESET}$					
Input High Voltage, V_{INH}	2.4			V	VDD = 3.3 V ± 10%
Input Current, I_{IN}		70	TBD	nA	Input=VDD=3.3V
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V ± 10%
Input Current, I_{IN}		-6.7	TBD	µA	Input = 0 V, VDD = 3.3 V
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS—$\overline{IRQ0}$, $\overline{IRQ1}$, MISO/HSD, CLKOUT, SYNC, VT_A, VT_B, VT_C, VT_N, ZX/$\overline{DREADY}$					VDD = 3.3 V ± 10%
Output High Voltage, V_{OH}	2.97			V	VDD = 3.3 V ± 10%
I_{SOURCE}			TBD	µA	
Output Low Voltage, V_{OL}			0.4	V	VDD = 3.3 V ± 10%
I_{SINK}			TBD	mA	
CF1, CF2, CF3/HSCLK					
Output High Voltage, V_{OH}	2.4			V	VDD = 3.3 V ± 10%
I_{SOURCE}			TBD	µA	
Output Low Voltage, V_{OL}			0.4	V	VDD = 3.3 V ± 10%
I_{SINK}			TBD	mA	
POWER SUPPLY					For specified performance
VDD Pin	2.97		3.63	V	Minimum = 3.3 V – 10%; maximum = 3.3 V + 10%
I_{DD}		10.8	TBD	mA	
		TBD	TBD	mA	When $\overline{RESET}$ pin is kept low.

[1] See the Typical Performance Characteristics section.
[2] See the Terminology section for a definition of the parameters.
[3] XTAL1/XTAL2 load capacitors refer to the capacitors that are mounted between the XTAL1 and XTAL2 pins of ADE7978 and GND. The capacitors should be chosen based on crystal manufacturer data sheet specification and they must not have more than the max value specified in the table.

ADE7978 TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, GND = DGND = 0 V, XTALIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C. Note that dual function pin names are referenced by the relevant function only within the timing tables and diagrams; see the ADE7978 Pin Configuration and Function Descriptions section for full pin mnemonics and descriptions.

Table 3. I²C-Compatible Interface Timing Parameter

		Standard Mode		Fast Mode		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time (Repeated) Start Condition	$t_{HD;STA}$	4.0		0.6		µs
Low Period of SCL Clock	t_{LOW}	4.7		1.3		µs
High Period of SCL Clock	t_{HIGH}	4.0		0.6		µs
Set-Up Time for Repeated Start Condition	$t_{SU;STA}$	4.7		0.6		µs
Data Hold Time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data Setup Time	$t_{SU;DAT}$	250		100		ns
Rise Time of Both SDA and SCL Signals	t_R		1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t_F		300	20	300	ns
Setup Time for Stop Condition	$t_{SU;STO}$	4.0		0.6		µs
Bus Free Time Between a Stop and Start Condition	t_{BUF}	4.7		1.3		µs
Pulse Width of Suppressed Spikes	t_{SP}	N/A[1]			50	ns

[1] N/A means not applicable.

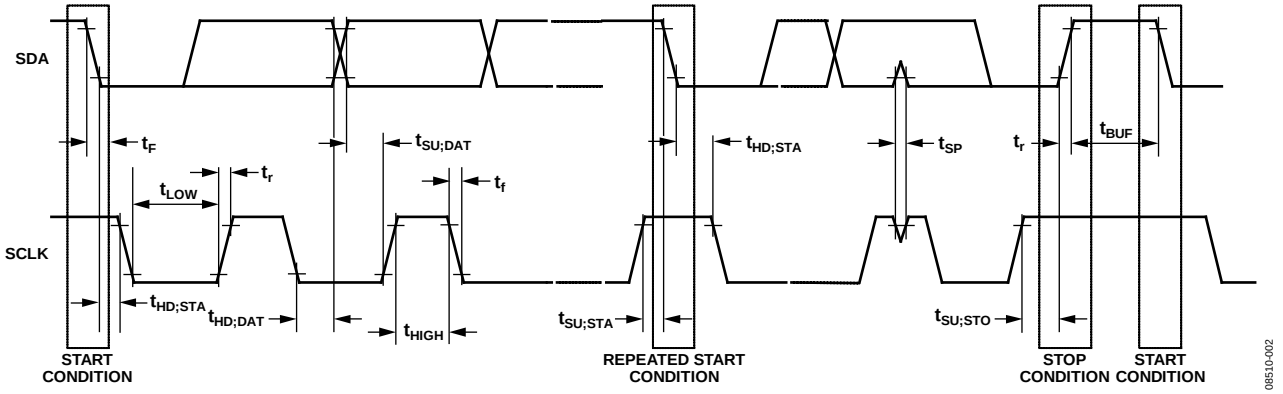


Figure 5. I²C-Compatible Interface Timing

Table 4. SPI Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	50		ns
SCLK Period		0.4	4000[1]	µs
SCLK Low Pulse Width	t_{SL}	175		ns
SCLK High Pulse Width	t_{SH}	175		ns
Data Output Valid After SCLK Edge	t_{DAV}		100	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	100		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	5		ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
SCLK Rise Time	t_{SR}		20	ns
SCLK Fall Time	t_{SF}		20	ns
MISO Disable After $\overline{SS}$ Rising Edge	t_{DIS}		200	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0		ns

[1] Guaranteed by design.

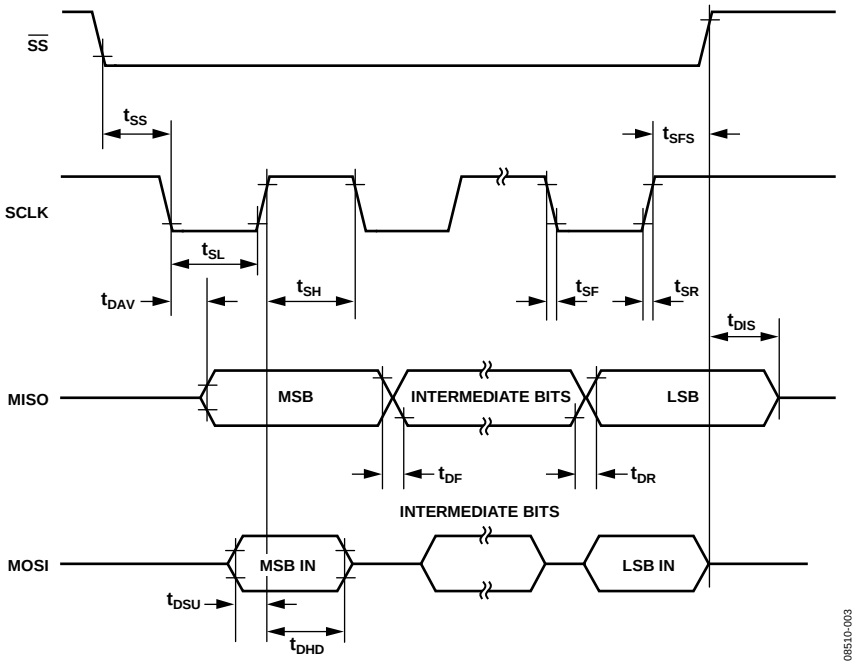


Figure 6. SPI Interface Timing

Table 5. HSDC Interface Timing Parameter

Parameter	Symbol	Min	Max	Unit
HSA to HSCLK Edge	t_{SS}	0		ns
HSCLK Period		125		ns
HSCLK Low Pulse Width	t_{SL}	50		ns
HSCLK High Pulse Width	t_{SH}	50		ns
Data Output Valid After HSCLK Edge	t_{DAV}		40	ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
HSCLK Rise Time	t_{SR}		10	ns
HSCLK Fall Time	t_{SF}		10	ns
HSD Disable After HSA Rising Edge	t_{DIS}	5		ns
HSA High After HSCLK Edge	t_{SFS}	0		ns

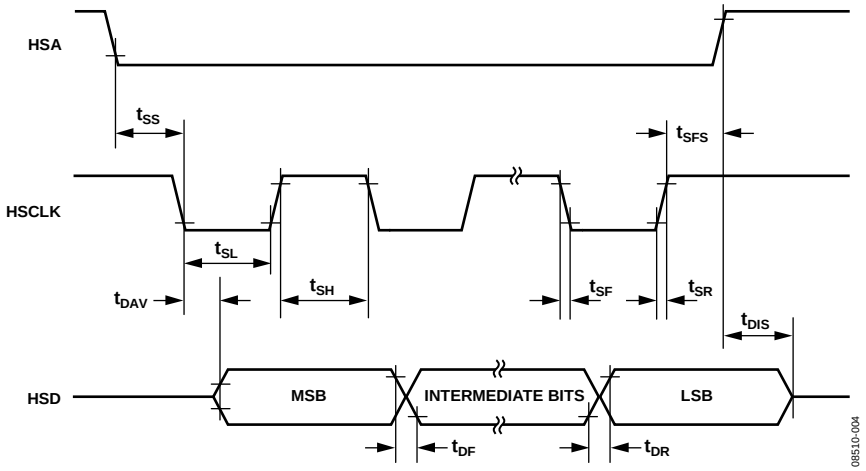


Figure 7. HSDC Interface Timing

Table 6. Bit Stream Interface Timing Parameter

Parameter	Symbol	Min	Max	Unit
XTAL1 low pulse width	t_{SH}			
XTAL1 high pulse width	t_{SL}			
XTAL1 fall time	t_{SF}			
XTAL1 rise time	t_{SR}			
SYNC high valid before XTAL1 high to low edge	t_{SHV}			
SYNC low valid before XTAL1 high to low edge	t_{SLV}			
DATA_A valid after XTAL1 high to low edge	t_{DV}			
DATA_A rise time	t_{DR}			
DATA_A fall time	t_{DF}			

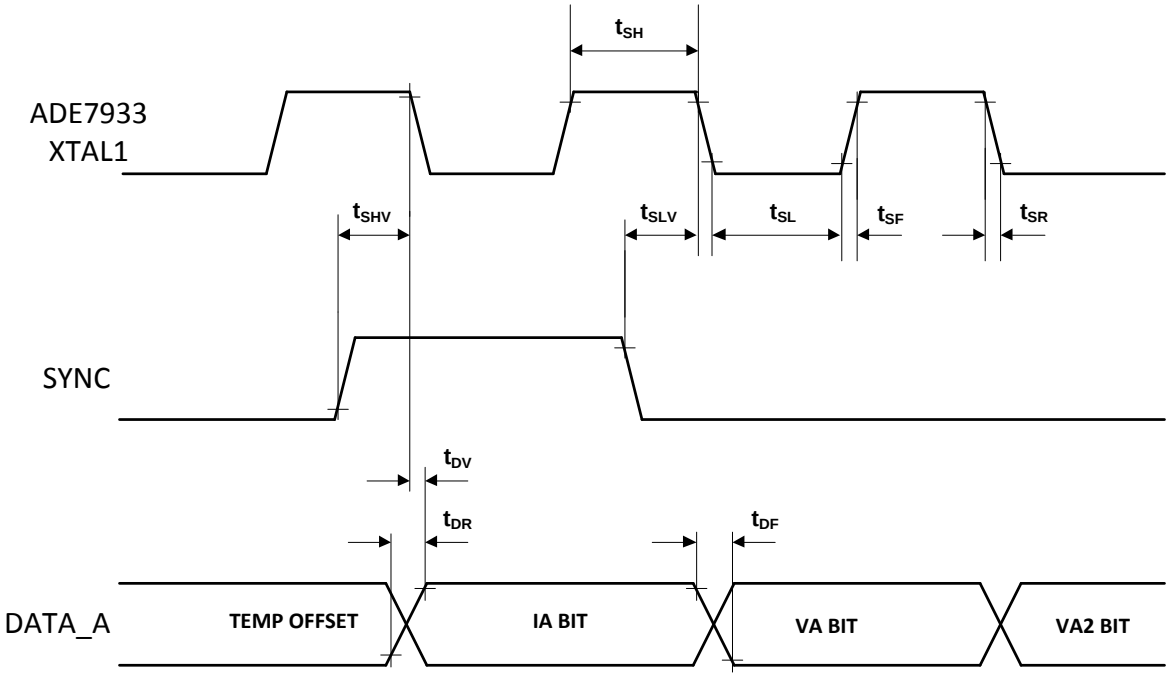


Figure 8. Bit Stream Interface Timing

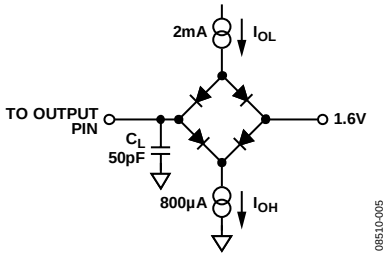


Figure 9. Load Circuit for Timing Specifications

ADE7978 ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
VDD to GND	−0.3 V to +3.7 V
Digital Input Voltage to DGND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C

Note: Regarding the temperature profile used in soldering RoHS Compliant Parts : Analog Devices advises reflow profiles should conform to J-STD 20 from JEDEC. Refer to www.jedec.org for latest revision.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified equal to 29.3°C/W; θ_{JC} is specified equal to 1.8°C/W.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
28-Lead LFCSP	29.3	1.8	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADE7933/ADE7932 SPECIFICATIONS

V_{DD1} = 3.3 V ± 10%, GND = 0 V, on-chip reference, CLKIN = 4.096 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_{TYP}= 25°C.

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG INPUTS					
Differential Signal Levels at IP pin with regard to IM pin			±31.25	mV peak	IM pin is connected to GND_{ISO}.
Pseudo Differential Signal at V1P and V2P pins with regard to VM pin			±500	mV peak	Pseudo differential inputs between V1P and VM pins and between V2P and VM pins. VM pin is connected to GND_{ISO}.
Maximum common-mode voltage			±25	mV	
Integral Linearity Error	-TBD	±TBD	+TBD	LSB	
Crosstalk		TBD	TBD	dB	One input set to GND_{ISO}, all other inputs at full scale
Input Impedance (DC)					
IP, IM, V1P, and V2P Pins	TBD			kΩ	
VM Pin	TBD			kΩ	
ADC Offset Error		TBD		mV	Uncalibrated error, see the TBD section
ADC Offset Drift over temperature			±TBD	nV/°C	
Gain Error			±TBD	%	
Gain Drift over temperature			±TBD	ppm of FS/°C	
AC Power Supply Rejection	TBD	TBD		dB	VDD = 3.3 V + 120 mV rms/120 Hz, IP = ±6.25mV rms, V1P = V2P = ± 100mV rms
DC Power Supply Rejection	TBD	TBD		dB	VDD=3.3 V ± 330 mV dc, IP = ±6.25mV rms, V1P = V2P = ± 100mV rms
Temperature Sensor					
Accuracy		±5		°C	
ON-CHIP REFERENCE					Nominal TBD V at the $REF_{IN/OUT}$ pin at T_A = 25°C
Reference Error			±2	mV max	
Output Impedance	1.2			kΩ min	
Temperature Coefficient		10	50	ppm/°C	
CLOCK INPUT					
Input Clock Frequency XTAL1		4.096		MHz	Provided by the ADE7978
XTAL1 Duty Cycle	45	50	55	%	If used without ADE7978
XTAL1 logic inputs					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	
Crystal Equivalent Series Resistance	30		200	Ω	
XTAL1 Load Capacitor		20	40	pF	
XTAL2 Load Capacitor		20	40	pF	
LOGIC INPUTS—SYNC,V2/ $\overline{\text{TEMP}}$, $\overline{\text{RESET\_EN}}$					
Input High Voltage, V_{INH}	2.4			V	VDD = 3.3 V ± 10%
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V ± 10%
Input Current, I_{IN}			±3	µA	Typical 10nA, V_{IN}=0V to VDD
Input Capacitance, C_{IN}			10	pF	

Notes:

See the Terminology section for a definition of the parameters.

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS—DATA					VDD = 3.3 V ± 10%

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output High Voltage, V_{OH}	3.0			V	I_{SOURCE}=800µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK}=2mA
POWER SUPPLY					For specified performance
V_{DD} Pin	3.0		3.6	V	Minimum = 3.3 V – 10%; maximum = 3.3 V + 10%
I_{DD}		TBD	TBD	mA	
		TBD	TBD	mA	When XTAL1 input is kept high.

REGULATORY APPROVALS

Table 11. Regulatory Approvals

UL Pending	CSA	VDE (Pending)
Recognized under 1577 component recognition program	Approved under CSA Acceptance Notice #5A	Certified according to DIN VDE V 0884-10 (VDE V 0884-10):2006-12
5000 V rms isolation voltage single protection	Basic insulation per IEC 61010-1, 400 V rms (564 V peak) maximum working voltage	Reinforced insulation, 846 V peak
File TBD	File TBD	File TBD

Notes:

In accordance with UL 1577, each ADE7933/ADE7932 is proof tested by applying an insulation test voltage ≥ 6000V rms for 1 second (current leakage detection limit = 10µA).

In accordance with DIN EN 60747-5-2, each ADE7933/ADE7932 is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 second (partial discharge detection limit = 5pC).

In accordance with DIN V VDE V 0884-10, each ADE7933/ADE7932 is proof tested by applying an insulation test voltage ≥ 1590 peak for 1 second (partial discharge detection limit = 5pC). The * marking branded on the component designates DIN V VDE 0884-10 approval.

INSULATION AND SAFETY

Table 12. Critical Safety-Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(l01)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(l02)	>8.3	mm	Measured from input terminals to output terminals, shortest distance through path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Distance through insulation
Tracking resistance (Comparative Tracking index)	CTI	>400	V	IEC 60112
Isolation Group		II		Material group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

The ADE7913 is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits. The asterisk (*) marking on packages denotes DIN V VDE V 0884-10 approval.

Table 13. VDE Characteristics

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	846	V peak
Input-to-Output Test Voltage, Method b1	V_{IORM} x 1.875=V_{PR}, 100% production test, t_m=1 sec, partial discharge < 5pC	V_{PR}	1590	V peak
Input-to-Output Test Voltage, Method a		V_{PR}		
After Environmental Tests Subgroup 1	V_{IORM} x 1.6=V_{PR}, t_m=60 sec, partial discharge < 5pC		1375	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} x 1.2=V_{PR}, t_m=60 sec, partial discharge < 5pC		1018	V peak
Highest allowable Overvoltage	Transient overvoltage, t_{TR}=10sec	V_{TR}	6000	V peak
Safety limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Side 1 I_{DD} Current		I_S	TBD	mA
Insulation Resistance at Ts	V_{IO}=500V	R_S	$>10^9$	Ω

TBD

Figure 10. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN 60747-5-2

ADE7933/ADE7932 ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 14.

Parameter	Rating
V_{DD} to GND	−0.3 V to +3.7 V
Analog Input Voltage to GND_{ISO}, IP, IM, V1P, V2P, VM	−2 V to +2 V
Reference Input Voltage to GND_{ISO}	−0.3 V to VDD + 0.3 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.3 V
Common-Mode Transients	-100 kV/µs to +100 kV/µs
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	TBD
Lead Temperature (Soldering, 10 sec)	TBD

Note: Regarding the temperature profile used in soldering RoHS Compliant Parts : Analog Devices advises reflow profiles should conform to J-STD 20 from JEDEC. Refer to www.jedec.org for latest revision.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified equal to 48.0 °C/W; θ_{JC} is specified equal to 6.2 °C/W.

Table 15. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead SOIC	48.0	6.2	°C/W

ESD CAUTION

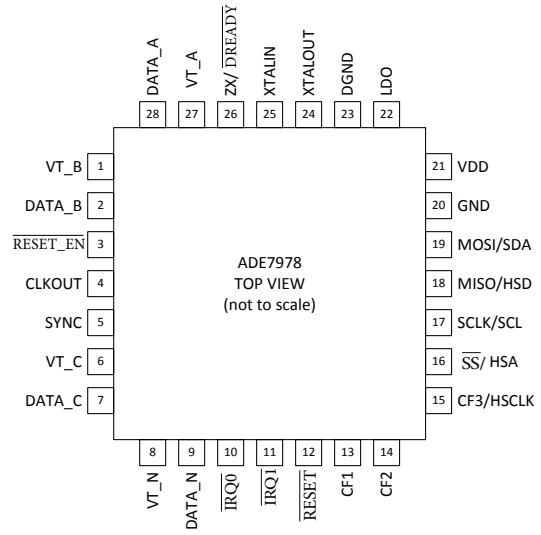
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 16. Maximum Continuous Working Voltage Supporting 50-Year Minimum Lifetime[1]

Parameter	Max	Unit	Applicable Certification
AC Voltage, Bipolar Waveform	564	V peak	All certifications, 50-year operation
AC Voltage, Unipolar Waveform			
Basic Insulation	TBD	V peak	
Reinforced Insulation	TBD	V peak	Working voltage per IEC 61010-1
DC Voltage			
Basic Insulation	TBD	V peak	
Reinforced Insulation	TBD	V peak	Working voltage per IEC 61010-1

[1]Refers to the continuous voltage magnitude imposed across the isolation barrier. See Insulation Lifetime section for more details

ADE7978 PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTE
CREATE A SIMILAR PAD ON THE PCB UNDER THE EXPOSED PAD. SOLDER THE EXPOSED PAD TO THE PAD ON THE PCB TO CONFER MECHANICAL STRENGTH TO THE PACKAGE. CONNECT THE PAD TO DGND.

Figure 11. Pin Configuration

Table 17. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VT_B	Selects V2P or the temperature measurement on the Phase B ADE7933/ADE7932. Connect this pin to V2/ $\overline{\text{TEMP}}$ pin of the Phase B ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense the phase B, like in the 3-phase 3-wire delta configuration case, leave this pin unconnected.
2	DATA_B	Receives the bit streams from the Phase B ADE7933/ADE7932.Connect this pin to DATA pin of the Phase B ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense the phase B, like in the 3-phase 3-wire delta configuration, connect this pin to VDD.
3	$\overline{\text{RESET\_EN}}$	Reset Output Enable. Connect this pin to $\overline{\text{RESET\_EN}}$ pin of the ADE7933/ADE7932s. See Hardware Reset on how this pin is used by the ADE7978 to reset the ADE7933/ADE7932s.
4	CLKOUT	4.096MHz output clock signal. Connect this pin to the XTAL1 pin of the ADE7933/ADE7932s.
5	SYNC	Clock output (4.096 MHz) used as serial clock of the serial communication with the ADE7933/ADE7932. Connect this pin to SYNC pin of the ADE7933/ADE7932s.
6	VT_C	Selects V2P or the temperature measurement on the Phase C ADE7933/ADE7932. Connect this pin to V2/$\overline{\text{TEMP}}$ pin of the Phase C ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense the phase C, leave this pin unconnected.
7	DATA_C	Receives the bit streams from the Phase C ADE7933/ADE7932. Connect this pin to DATA pin of the Phase C ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense the phase C, connect this pin to VDD.
8	VT_N	Selects V2P or the temperature measurement on the neutral line ADE7933/ADE7932. Connect this pin to V2/$\overline{\text{TEMP}}$ pin of the neutral line ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense the neutral line, leave this pin unconnected.
9	DATA_N	Receives the bit streams from neutral line ADE7933/ADE7932. Connect this pin to DATA pin of the neutral line ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense the neutral line, connect this pin to VDD.
10, 11	$\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$	Interrupt Request Outputs. These are active low logic outputs. See the Interrupts section for a detailed presentation of the events that can trigger interrupts.
12	$\overline{\text{RESET}}$	Reset Input, Active Low.This pin should stay low for at least 10µs to trigger a hardware reset.
13, 14, 15	CF1, CF2, CF3/HSCLK	Calibration Frequency (CF) Logic Outputs. These outputs provide power information and are used for operational and calibration purposes. CF3 is multiplexed with the serial clock output of the HSDC port.

Pin No.	Mnemonic	Description
16	$\overline{SS}$/HSA	Slave Select for SPI Port/HSDC Port Active.
17	SCLK/SCL	Serial Clock Input for SPI Port/Serial Clock Input for I^2C Port. This pin has a Schmidt trigger input for use with a clock source that has a slow edge transition time, for example, opto-isolator outputs.
18	MISO/HSD	Data Out for SPI Port/Data Out for HSDC Port.
19	MOSI/SDA	Data In for SPI Port/Data Out for I^2C Port.
20	GND	Ground Reference. This pin provides the ground reference for the analog circuitry.
21	VDD	Supply Voltage. This pin provides the supply voltage. Maintain the supply voltage at 3.3 V ± 10% for specified operation. Decouple this pin to GND with a 10µF capacitor in parallel with a ceramic 100nF capacitor.
22	LDO	1.8 V output of the digital low dropout regulator (LDO). Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor. Do not connect external active circuitry to this pin.
23	DGND	Ground Reference. This pin provides the ground reference for the digital circuitry.
24	XTALOUT	A crystal can be connected across this pin and XTALIN (as previously described with Pin 24 in this table) to provide a clock source for the ADE7978.
25	XTALIN	Master Clock. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT-cut crystal can be connected across XTALIN and XTALOUT to provide a clock source for the ADE7978. The clock frequency for specified operation is 16.384 MHz. Use ceramic load capacitors of a few tens of picofarad with the gate oscillator circuit. Refer to the crystal manufacturer's data sheet for load capacitance requirements.
26	ZX/$\overline{DREADY}$	Zero Crossing (ZX) output pin. ZX pin goes high on the positive-going edge of the selected phase voltage zero crossing and low on the negative-going edge of the zero crossing (see Zero-Crossing Detection for details). $\overline{DREADY}$ is an active low signal generated 6.5µs before bit 17 (DREADY) in STATUS0 register is set to 1. It has 8 kHz frequency and stays low for 10 µsec every period.
27	VT_A	Selects V2P or temperature measurement on Phase A ADE7933/ADE7932. This pin should be connected to pin V2/$\overline{TEMP}$ of the Phase A ADE7933/ADE7932. Connect this pin to V2/$\overline{TEMP}$ pin of the Phase A ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense the phase A, leave this pin unconnected.
28	DATA_A	Receives the bit streams from Phase A ADE7933/ADE7932. Connect this pin to DATA pin of the Phase A ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense the phase A, connect this pin to VDD.
EP	Exposed Pad	Create a similar pad on the PCB under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package. Connect the pads to DGND.

ADE7933/ADE7932 PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

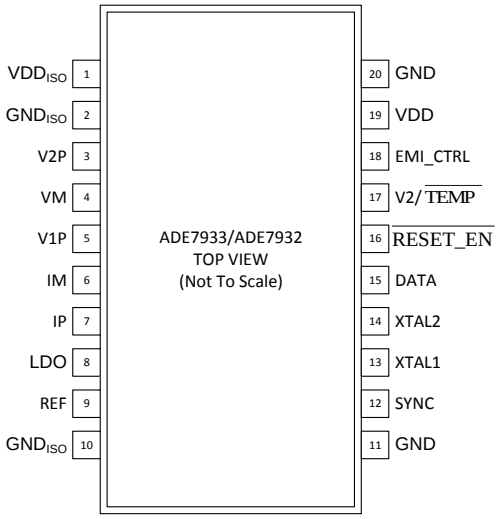


Figure 12. ADE7933/ADE7932 Pin Configuration

Table 18. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD_{ISO}	This pin provides access to the 3.3V on-chip isolated power supply. Do not connect external active circuitry to this pin. Decouple this pin with a 10 µF capacitor in parallel with a ceramic 0.1 µF capacitor.
2,10	GND_{ISO}	Ground Reference of the isolated secondary side. This pin provides the ground reference for the analog circuitry. Use this quiet ground reference for all analog circuitry.
3,4,5	V2P, VM, V1P	Analog Inputs for the Voltage Channels. These channels are used with the voltage transducers and are referenced as the Voltage Channels in this document. These inputs are single-ended voltage inputs with a maximum signal level of ±0.5 V with respect to VM for specified operation. If not used, connect V1P or V2P pins to VM pin. On the ADE7932, connect V2P pin to VM pin as V2P voltage channel is not available.
6,7	IM, IP	Analog Inputs for Current Channel. This channel is used with shunts and is referenced in this document as Current Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±31.25 mV.
8	LDO	2.5V output of the analog low dropout regulator (LDO). Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 0.1µF capacitor. Do not connect external active circuitry to this pin.
9	REF	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V. Decouple this pin to GND_{ISO} with a 4.7 µF capacitor in parallel with a ceramic 0.1µF capacitor.
11,20	GND	Primary ground reference.
12	SYNC	Clock signal of 4.096 MHz generated by the ADE7978 used for the serial communication between the ADE7933/ADE7932 and ADE7978. Connect SYNC pin to SYNC pin of the ADE7978.
13	XTAL1	Master Clock. Connect this pin to the ADE7978 CLKOUT pin. The clock frequency for specified operation is 4.096 MHz. Do not clock the ADE7933/ADE7932s using a crystal connected between XTAL1 and XTAL2 pins because the ADE7933/ADE7932s must function synchronously with the ADE7978 and only CLKOUT clock ensures this.
14	XTAL2	Leave this pin open.
15	DATA	Data Output for communication with the ADE7978. Connect DATA pin to one of the DATA_A, DATA_B, DATA_C or DATA_N pins of the ADE7978. Connect the DATA pin of the Phase A ADE7933/ADE7932 to DATA_A pin of the ADE7978, etc.
16	$\overline{\text{RESET\_EN}}$	Reset Input Enable, Active Low. The ADE7933/ADE7932 is reset by setting $\overline{\text{RESET\_EN}}$ pin low and toggling 4 times VB/$\overline{\text{TEMP}}$ pin with a frequency of 4.096 MHz. The reset ends when this pin and VB/$\overline{\text{TEMP}}$ pin are set high.
17	V2/$\overline{\text{TEMP}}$	Input pin that selects which signal is converted at the second voltage channel of the ADE7933/ADE7932. It is also used during ADE7933/ADE7932 reset procedure. If it is high, voltage V2P input is sensed. If it is low, the temperature sensor is measured. Always connect V2/$\overline{\text{TEMP}}$ pin of to one of VT_A, VT_B, VT_C or VT_N pins of the ADE7978. Connect V2/$\overline{\text{TEMP}}$ pin of the Phase A

Pin No.	Mnemonic	Description
		ADE7933/ADE7932 to VT_A pin of the ADE7978, etc.
18	EMI_CTRL	This pin manages the emissions of the ADE7933/ADE7932. When the pin is connected to GND, the dc-to-dc converter is controlled and thus emits during slots 0, 2, 4, and 6. When the pin is connected to VDD, the the dc-to-dc converter is controlled and thus emits during slots 1, 3, 5, and 7. See DC-TO-DC CONVERTER section for more details). Do not leave the pin floating.
19	VDD	Primary Supply Voltage. This pin provides the supply voltage of the ADE7933/ADE7932. Maintain the supply voltage at 3.3 V ± 10% for specified operation. Decouple this pin to GND with a 10 µF capacitor in parallel with a ceramic 0.1 µF capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

TBD

TEST CIRCUIT

TBD

Figure 13. Test Circuit

TERMINOLOGY

Integral Nonlinearity (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. The deviation is measured from the middle of each code to the true straight line.

ADC Offset Error
This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the input range of each channel.

Gain Error
The gain error in the ADCs of the ADE7933/ADE7932 is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code (see Current Channel ADC and Voltage Channel ADCs sections). The difference is expressed as a percentage of the ideal code.

Power Supply Rejection (PSR)
This quantifies the ADE7978 and ADE7933/ADE7932 chipset measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms at 100 Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading (Power Supply Rejection Ratio, PSRR). Then PSR= 20 $\log_{10}$ (PSRR).

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied ±10%. Any error introduced is expressed as a percentage of the reading (PSRR). Then PSR= 20 $\log_{10}$ (PSRR).

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Measurement Error
The error associated with the energy measurement made by the ADE7978 and ADE7933/ADE7932 chipset is defined by

$$Measurement\ Error = \frac{Energy\ Registered\ by\ ADE7978 - True\ Energy}{True\ Energy} \times 100\% \quad (1)$$

Power Supply Rejection (PSR)
This quantifies the ADE7978 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms at 100 Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading—see the Measurement Error definition.

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied ±10%. Any error introduced is expressed as a percentage of the reading.

CF Jitter

The period of pulses at one of the CF1, CF2, or CF3 pins is continuously measured. The maximum, minimum, and average values of four consecutive pulses are computed as follows:

$$Maximum = max(Period_0, Period_1, Period_2, Period_3)$$

$$Minimum = min(Period_0, Period_1, Period_2, Period_3)$$

$$Average = \frac{Period_0 + Period_1 + Period_2 + Period_3}{4}$$

The CF jitter is then computed as

$$CF_{JITTER} = \frac{Maximum - Minimum}{Average} \times 100\% \quad (2)$$

APPLICATION INFORMATION

The ADE7978 and ADE7933/ADE7932 chipset has been designed to be used in three-phase energy metering systems in which one master device, usually a microcontroller, manages ADE7978 through an I2C or SPI interface. The ADE7978 then manages two, three or four ADE7933s/ADE7932.

The ADE7978 is not the only chip capable of managing multiple ADE7933/ADE7932s. Any microcontroller that conforms to the ADE7933/ADE7932 serial interface may manage them correctly (see Bit-Stream Communication between ADE7978 and ADE7933/ADE7932 for more details). The ADE7913/ADE7912, the 3-channel, isolated, sigma delta ADC, is similar to the ADE7933/ADE7932 and has a SPI interface. This makes it more suitable to being interfaced directly with a microcontroller. See www.analog.com for more details.

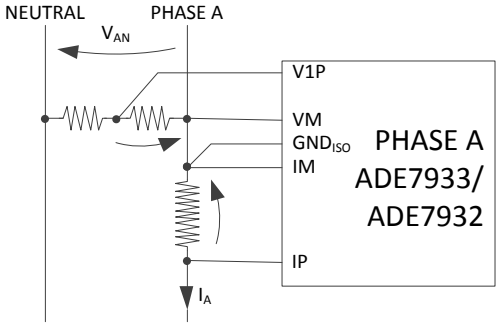


Figure 14. Phase A ADE7933/ADE7932 current and voltage sensing

Figure 14 presents the phase A of a three phase energy meter. The phase A current, I_A, is sensed with a shunt. A pole of the shunt is connected to IM pin of the ADE7933/ADE7932 and becomes the ground of the isolated side of the ADE7933/ADE7932, GND_{ISO}. The phase A to neutral voltage V_{AN} is sensed with a resistor divider and VM pin is also connected to IM and GND_{ISO} pins. Note that the voltages measured by the ADCs of the ADE7933/ADE7932 are opposite to V_{AN} and I_A, a classic approach of single phase metering. The other ADE7933/ADE7932s that monitor phases B and C are connected in a similar way.

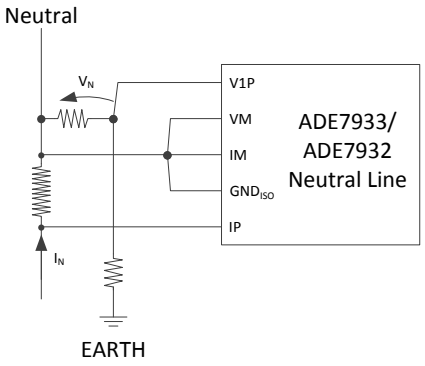


Figure 15. Neutral Line and Neutral to Earth Voltage Monitoring with ADE7933/ADE7932

Figure 15 presents how the ADE7933/ADE7932 inputs are connected when the neutral line of a three-phase system is monitored. The neutral current is sensed using a shunt and the voltage across the shunt is measured at the fully differential inputs IP and IM. The earth to neutral voltage is sensed with a voltage divider at the single ended inputs V1P and VM.

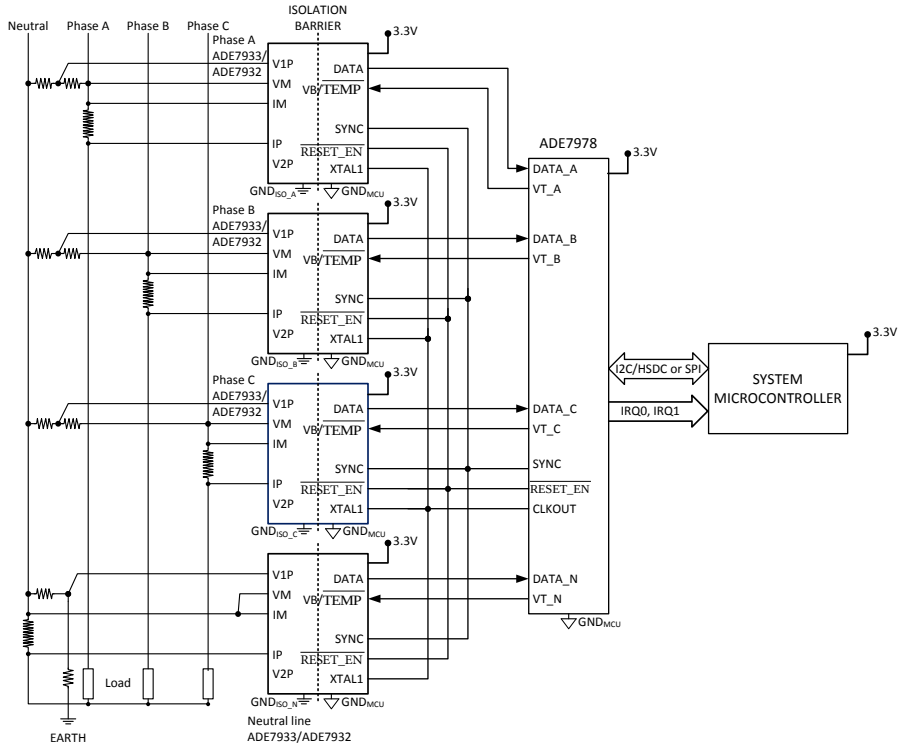


Figure 16. Three phase 4-wire wye meter with one ADE7978 and four ADE7933s

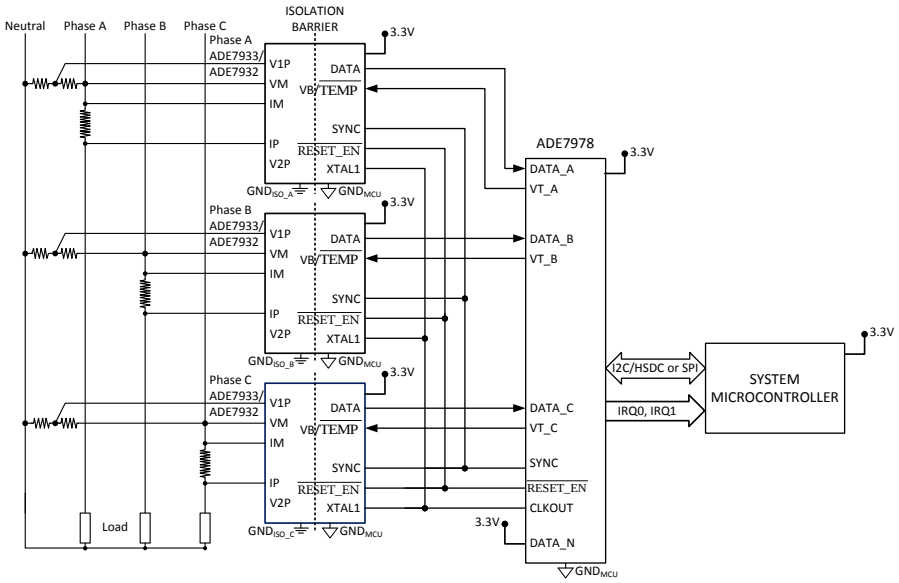


Figure 17. Three phase 4-wire wye meter with one ADE7978 and three ADE7933/ADE7932s

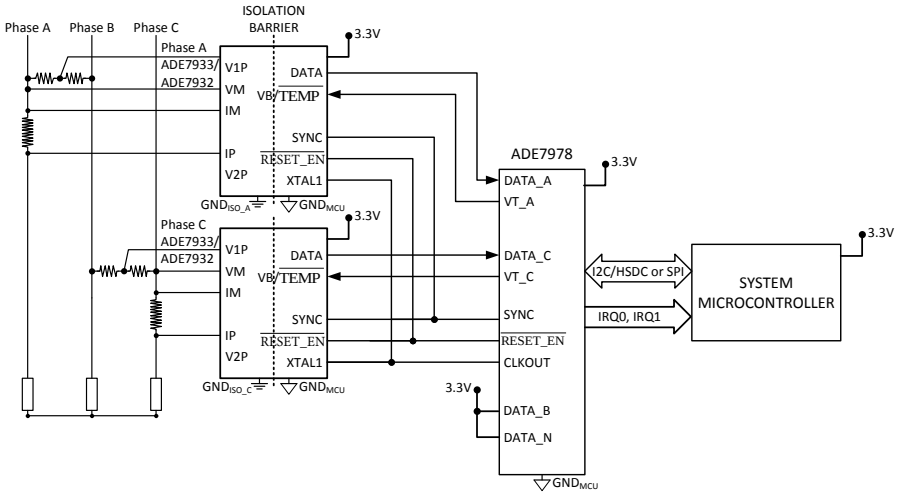


Figure 18. Three phase 3-wire delta meter with one ADE7978 and two ADE7933ADE7932s

ADE7978 AND ADE7933/ADE7932 IN POLY-PHASE ENERGY METERS

A poly-phase energy meter must manage three phases and an eventual neutral line. Figure 1 and Figure 16 present an example of a three phase meter built for a 4-wire wye configuration. Three ADE7933/ADE7932s read the phase currents and voltages. The fourth ADE7933/ADE7932 manages the neutral line measurements. If the neutral line measurements are not required, then only three ADE7933/ADE7932s are used (Figure 17). DATA_N pin of the ADE7978 is connected to VDD in this case. If the meter is built for 3-wire delta configuration, only two ADE7933/ADE7932s are required (Figure 18): one for phase A and one for phase C. The voltage dividers measure the phase A to B and the phase C to B voltages. The shunts measure the phase A and C currents. DATA_N and DATA_B pins of the ADE7978 are connected to VDD in this case.

If only two or three ADE7933/ADE7932s are used, DATA_B and/or DATA_N are connected to VDD. The waveform samples computed by the ADE7978 that correspond to these unconnected ADE7933/ADE7932s are set to full scale. After passing through the high pass filter, the waveform samples are set to 0 and all quantities computed by the ADE7978 using them are 0.

The ADE7933/ADE7932s receive a 4.096MHz clock at XTAL1 pins from the ADE7978 pin CLKOUT. In this case, the XTAL2 pins of the ADE7933/ADE7932s are left open. Do not clock the ADE7933/ADE7932s using a crystal connected between XTAL1 and XTAL2 pins because the ADE7933/ADE7932s must function synchronously with the ADE7978 and only CLKOUT clock ensures this.

The ADE7978 $\overline{\text{RESET\_EN}}$ pin is connected to the $\overline{\text{RESET\_EN}}$ pins of all ADE7933/ADE7932s of the system. The ADE7978 VT_A, VT_B, VT_C and VT_N pins are connected to the corresponding VB/$\overline{\text{TEMP}}$ pin of every ADE7933/ADE7932 of the system. For example, the VT_A pin of the ADE7978 is

connected to VB/$\overline{\text{TEMP}}$ pin of the ADE7933/ADE7932 that monitors the phase A. If the schematic does not monitor certain phases, leave the corresponding VT_x pins of the ADE7978 unconnected. For example, the meter in Figure 18 configuration does not monitor phase B and the neutral current. Therefore, pins VT_B and VT_N are left open.

When the $\overline{\text{RESET}}$ pin of the ADE7978 is set low for at least 10µs and then is brought high, the $\overline{\text{RESET\_EN}}$ pin is set low and VT_A, VT_B, VT_C and VT_N pins toggle 8 times high low with a frequency of 4.096 MHz, resetting the ADE7933/ADE7932s. Then $\overline{\text{RESET\_EN}}$, VT_A, VT_B, VT_C and VT_N pins are set high and the reset of the ADE7933/ADE7932s ends (see Hardware Reset section for more details).

The pins VT_A, VT_B, VT_C and VT_N of the ADE7978 select the signal measured by the V2 voltage ADC of the ADE7933/ADE7932. If the VT_x signal is low, the ADC measures the input signal at pin V2P. If the signal is high, the ADC measures the internal temperature sensor.

The ADE7978 reads the ADE7933/ADE7932s outputs using a bit stream communication composed of two signals, SYNC and DATA. SYNC pin of the ADE7978 is connected to SYNC pins of all ADE7933/ADE7932s. The DATA pin of every ADE7933/ADE7932 is connected to a corresponding DATA_x (x=A, B, C and N) pin of the ADE7978. For example, the DATA pin of the Phase A ADE7933/ADE7932 is connected to DATA_A pin of the ADE7978. If the schematic does not monitor certain phases, connect corresponding DATA_x pins of the ADE7978 to VDD. For example, the meter in Figure 18 configuration does not monitor phase B and the neutral current. Therefore, the pins DATA_B and DATA_N of the ADE7978 are tied to VDD.

The SYNC pin of the ADE7978 generates a 1.024 MHz serial clock to the ADE7933/ADE7932s slaves. Every ADE7933/ADE7932 responds with a bit stream generated by the first stage of the ADE7933/ADE7932 ADCs (see Bit-Stream Communication between ADE7978 and ADE7933/ADE7932 for more details).

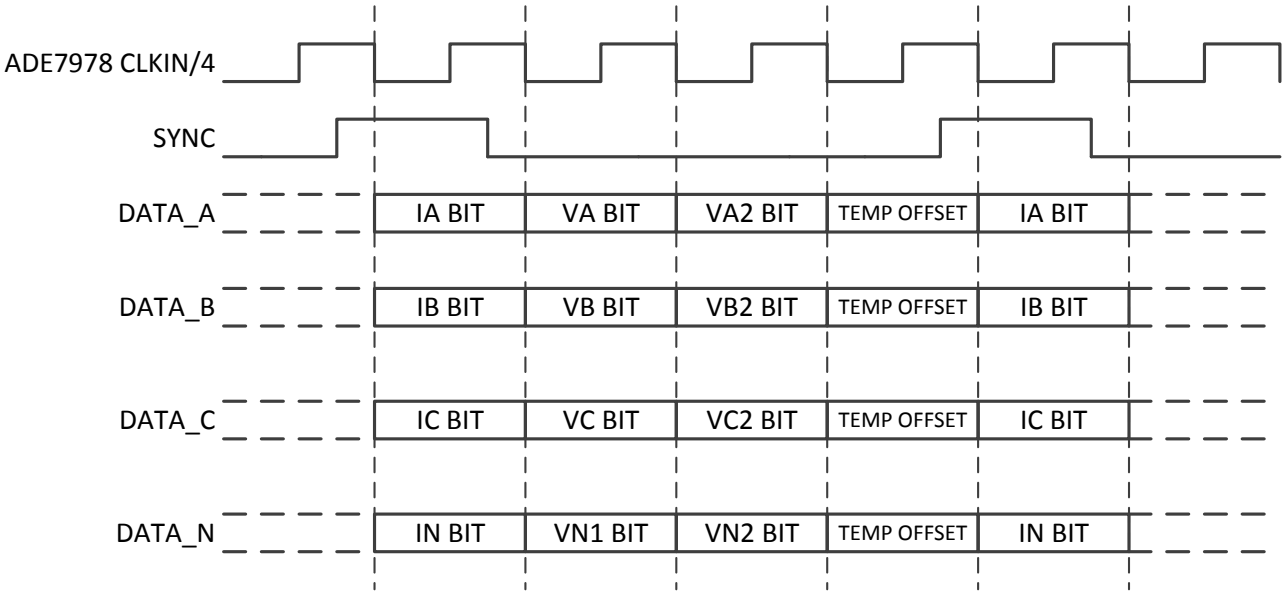


Figure 19. Bit stream communication between the ADE7978 and the ADE7933/ADE7932s

BIT-STREAM COMMUNICATION BETWEEN ADE7978 AND ADE7933/ADE7932

The ADE7978 extracts the information from the ADE7933/ADE7932s of the system using the bit stream communication illustrated in Figure 19. The ADE7978 generates at SYNC pin a clock signal equal to one 16th of its internal clock, CLKIN/16 (1.024 MHz for XTALIN=16.384 MHz) and one fourth of the ADE7933/ADE7932 XTAL1 clock (CLKIN/4). The duty cycle is 25%.

The low to high transition of SYNC is generated one fourth of a cycle before a high to low transition of the CLKIN/4 clock. SYNC stays high for one CLKIN/4 cycle. It stays low for the rest of the period. After the first low to high transition of SYNC, when the ADE7978 CLKIN/4 has the high to low transitions, the ADE7933/ADE7932s put at the DATA pin the bits coming out from the first stage of the ADCs together with the bits of the temperature offset stored into the ADE7933/ADE7932s. The ADE7978 receives these bits at its DATA_A, DATA_B, DATA_C and DATA_N pins. Then the process repeats when SYNC has a new low to high transition.

Any master device that can generate a 1.024 MHz SYNC signal like in Figure 19 and filter the bit streams coming from DATA pins of the ADE7933/ADE7932s may replace the ADE7978.

POWER MANAGEMENT

DC-TO-DC CONVERTER

The dc-to-dc converter section of the ADE7933/ADE7932 works on the principles that are common to most modern power supply designs. V_{DD} power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. Power is transferred to the secondary side where it is rectified to a high dc voltage. The power is then linearly regulated down to about 3.3V and supplied to the ADC side section through a 2.5V LDO regulator.

The ADE7933/ADE7932's internal dc-to-dc converter state is controlled by the input V_{DD}. In normal operation mode, V_{DD} should be maintained between 2.97V and 3.63V.

The block diagram of the isolated dc-to-dc converter is presented in Figure 20. The ADE7933/ADE7932 primary supply voltage VDD input supplies an alternative current (ac) source. The ac signal passes through a chip-scale air core transformer and it is transferred to the secondary side. A rectifier then produces the isolated power supply VDD_{ISO}. Using another chip-scale air core transformer, a feedback circuit measures VDD_{ISO} and passes the information back into the VDD domain where a PWM control block controls the ac source to maintain VDD_{ISO} at 3.3V.

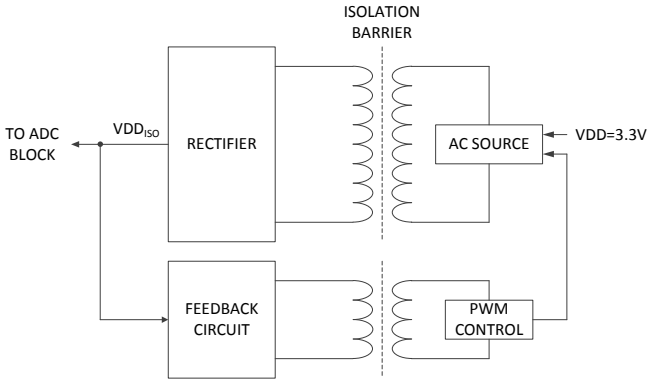


Figure 20. Isolated dc-to-dc Converter Block Diagram

The PWM control block works at CLKIN/4 (1.024 MHz) clock and every other half period generates a PWM pulse to the ac source based on the state of EMI_CTRL pin (Figure 21).

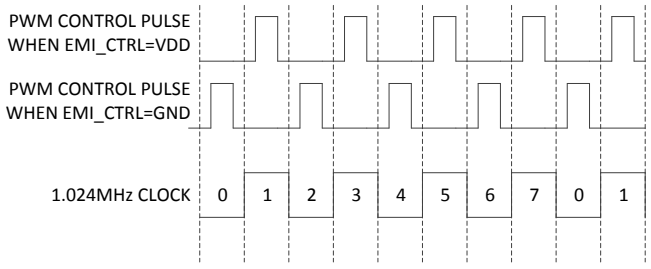


Figure 21. PWM Control Block Generates Pulses Based on 1MHz Clock

Every time a PWM pulse is generated, the ac source transmits very high frequency signals across the isolation barrier to allow efficient power transfer through the small chip-scale transformers. This creates high frequency currents that can propagate in circuit board ground and power planes, causing edge and dipole radiation. The PCB Board Layout section presents the best PCB layout approach to deal with the electromagnetic interference (EMI) issues. In addition to the layout approach, the EMI_CTRL pin helps in reducing the emissions generated by the ADE7913 dc-to-dc converter.

Every four periods of the clock that manages the PWM Control block are divided in 8 slots, 0 to 7, as presented in Figure 21.

When EMI_CTRL pin is connected to GND, the PWM Control block generates pulses during slots 0, 2, 4, and 6. When EMI_CTRL pin is connected to VDD, the PWM Control block generates pulses during slots 1, 3, 5, and 7.

If the three-phase energy meter contains four ADE7933/ADE7932s, use EMI_CTRL pin connected to GND for two of them and connected to VDD for the other two.

If the board contains three ADE7933/ADE7932s, use EMI_CTRL pin connected to GND for two of them and connected to VDD for the third.

If the board contains two ADE7933/ADE7932s, use EMI_CTRL pin connected to GND for one of them and connected to VDD for the other.

If the board contains one ADE7933/ADE7932s, use EMI_CTRL pin connected to GND.

MAGNETIC FIELD IMMUNITY

The ADE7933/ADE7932 is immune to dc magnetic fields because it uses air core transformers. The limitation on the ADE7933/ADE7932's ac magnetic field immunity is set by the condition in which the induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3.3V operating condition is examined because it is the nominal supply of the ADE7933/ADE7932.

The pulses at the transformer output have amplitude greater than 1.0V. The decoder has a sensing threshold at about 0.5V, thus establishing a 0.5V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = \left(-\frac{d\beta}{dt} \right) \sum_{n=1}^{N} \pi r_n^2 \qquad (3)$$

where:

β is the ac magnetic field: $\beta(t) = B \times \sin(\omega t)$

N is the number of turns in the receiving coil.

R_n is the radius of the n^{th} turn in the receiving coil.

Given the geometry of the receiving coil in the ADE7933/ADE7932 and an imposed requirement that the induced voltage V_{THR} be, at most, 50% of the 0.5V margin at the

decoder, a maximum allowable magnetic field B is calculated, as shown in Figure 22.

$$B = \frac{V_{THR}}{2\pi f \times \sum_{n=1}^{N} \pi r_n^2} \quad (4)$$

where f is the frequency of the magnetic field.

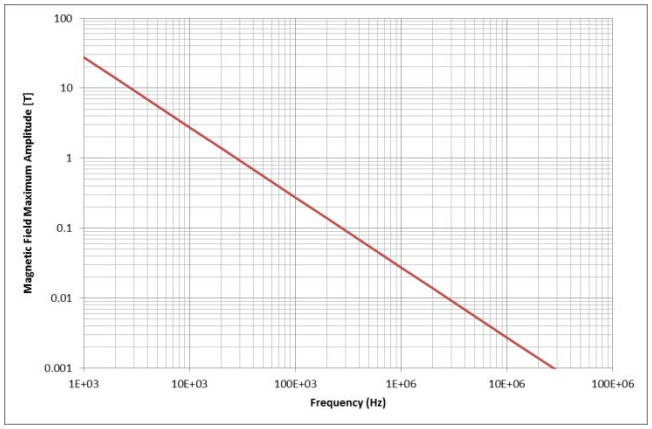


Figure 22. Maximum allowable external magnetic field

For example, at a magnetic field frequency of 10 kHz, the maximum allowable magnetic field of 2.8 T induces a voltage of 0.25V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from more than 1.0V to 0.75V, still well above the 0.5Vsensing threshold of the decoder.

The preceding magnetic field values correspond to specific current magnitudes at given distances from the ADE7933/ADE7932 transformers.

$$I = \frac{B}{\mu_0} \times 2\pi d = \frac{V \times d}{\mu_0 \times f \times \sum_{n=1}^{N} \pi r_n^2} \quad (5)$$

where μ_0 is $4\pi \times 10^{-7}$ H/m , the magnetic permeability ot the air.

Figure 23 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADE7933/ADE7932 is extremely immune and can be affected only be extremely large currents operated at high frequency very close to the component. For the 10 kHz example noted, one would have to place 5mm away from the ADE7933/ADE7932 a current with a magnitude of 69 kA to affect the component's operation.

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility (see PCB Board Layout section).

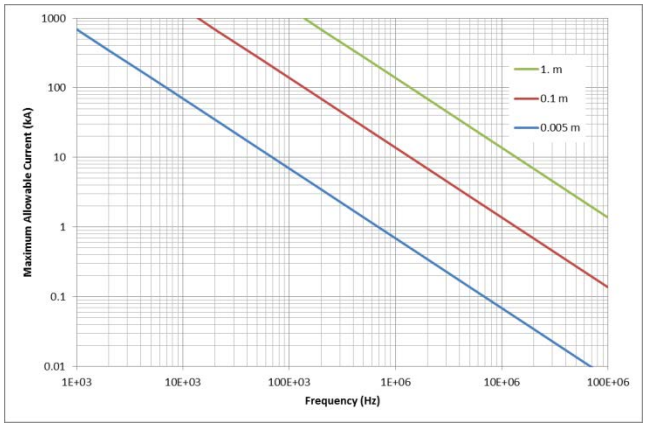


Figure 23. Maximum allowable current for various current-to-ADE7913 spacings

PCB BOARD LAYOUT

TBD

POWER UP PROCEDURE

The ADE7978 and ADE7933/ADE7932 chipset contains an on-chip power supply monitors that supervise the power supply (VDD). The ADE7933/ADE7932s have monitors with a threshold at 2.0V+/-10% and 23msec timeout timer. The ADE7978 has a monitor with a threshold between 2.5V and 2.6V and a timeout timer of 32 msec. As the ADE7933/ADE7932s are fully managed by the ADE7978, the power supply monitor of the ADE7978 is dominant and determinant. At power-up (see Figure 24), until VDD reaches a threshold between 2.5V to 2.6V, the ADE7978 is in an inactive state. This also keeps the ADE7933/ADE7932s in an inactive state. As VDD crosses this threshold, the ADE7978 power supply monitor keeps the chip in this inactive state for an additional 32 ms, allowing VDD to achieve 3.3 V – 10%, the minimum recommended supply voltage. Then the ADE7978 starts to function. The ADE7978 generates a 4.096MHz clock signal for the ADE7933/ADE7932s at CLKOUT pin, so the ADE7933/ADE7932s begin to function. After 10 ms, the ADE7978 resets the ADE7933/ADE7932s by setting $\overline{\text{RESET\_EN}}$ pin low and toggling 8 times high to low with 4.096 MHz frequency (CLKIN/4) the VT_A, VT_B, VT_C and VT_N pins. The ADE7933/ADE7932s begin to function at default conditions.

When the ADE7978 starts functioning after power up, the I^2C port is the active serial port. If the SPI port is used, then the $\overline{\text{SS}}$ /HSA pin must be toggled three times, high to low. This action selects the SPI port for further use. If I^2C is the active serial port, Bit 0 (I2C_LOCK) of the CONFIG2 register must be set to 1 to lock it in. From this moment, the ADE7978 ignores spurious toggling of the $\overline{\text{SS}}$/HSA pin, and an eventual switch to use the SPI port is no longer possible. Likewise, if SPI is the active serial port, any write to the CONFIG2 register locks the port, at which time a switch to use the I^2C port is no longer possible. Only a power-down or by setting the $\overline{\text{RESET}}$ pin low can the ADE7978 be reset to use the I^2C port.

Immediately after power up, the ADE7978 sets all registers to their default values.

The ADE7978 signals the moment in which itself and the ADE7933/ADE7932s become fully functional by triggering the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is 0 during the transition period and becomes 1 when the transition ends. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is returned high by writing the STATUS1 register with the corresponding bit set to 1. Because the RSTDONE is an unmaskable interrupt, Bit 15 (RSTDONE) in the STATUS1 register must be cancelled for the $\overline{\text{IRQ1}}$ pin to return high. It is recommended to wait until the $\overline{\text{IRQ1}}$ pin goes low before accessing the STATUS1 register to test the state of the RSTDONE bit. At this point, as a good programming practice, it is also recommended to cancel all other status flags in the STATUS1 and STATUS0 registers by writing the corresponding bits with 1.

Initially, the DSP is in idle mode, which means it does not execute any instruction. This is the moment to initialize all ADE7978 registers. First initialize the DSP RAM based registers located between addresses 0x4380 and 0x43BF. The last register in the queue must be written three times to ensure the register has been initialized. Then initialize the hardware based configuration registers located between addresses 0xE507 and 0xEA04. Then protect the integrity of the DSP RAM based configuration registers by writing 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3. Then write 0x0001 into the Run register to start the DSP (see the Digital Signal Processor section for details).

If the supply voltage, VDD, drops lower than 2 V ± 10%, the ADE7978 and the ADE7933/ADE7932s enter an inactive state, which means that no measurements or computations are executed.

The recommended actions at power up are:

-make sure the power supply ensures a transition from around 2.5 V, 2.6V to 3.3V-10% in less than 32msec.

-monitor $\overline{\text{IRQ1}}$ pin until it becomes low, meaning the RSTDONE interrupt is triggered..

-if SPI communication is used, toggle $\overline{\text{SS}}$/HSA pin three times, high to low to select it. If I²C communication is used, pass to the next step.

-read STATUS1 register, verify the bit 15 (RSTDONE) is set to 1 and then write it back. This ensures RSTDONE bit is cleared and $\overline{\text{IRQ1}}$ pin turns back high.

-If I²C communication is used, write CONFIG2 register with bit 0 (I2C_LOCK) set to 1 to lock the port in. If SPI communication is used, lock the port by writing any value to CONFIG2 register.

-Initialize all the ADE7978 registers. First initialize the DSP RAM based registers located between addresses 0x4380 and 0x43BF. Then write the last register in the queue three times. Then initialize the hardware based configuration registers located between addresses 0xE507 and 0xEA04.

-Enable the DSP RAM write protection by writing 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3. For more details, see Digital Signal Processor section.

-Write 0x0001 into the Run register to start the DSP.

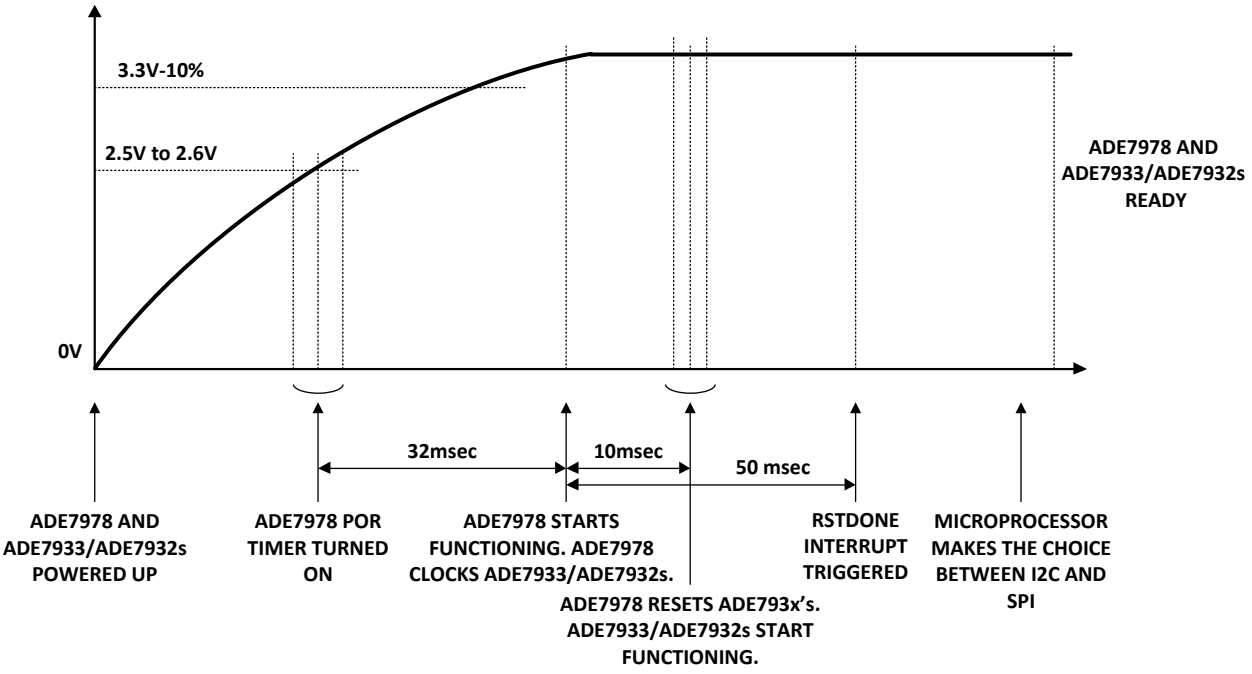


Figure 24. Power-Up Procedure

HARDWARE RESET

The ADE7978 has a $\overline{\text{RESET}}$ pin. If the $\overline{\text{RESET}}$ pin is set low, the ADE7978 enters the hardware reset state (see Figure 25). CLKOUT pin stops generating clock and is set high. SYNC, $\overline{\text{RESET\_EN}}$, VT_A, VT_B, VT_C and VT_N pins are set high. The dc-to-dc converter of the ADE7933/ADE7932s stops working because the clock signal at the ADE7933/ADE7932s XTAL1 pin is high. The sigma delta modulators placed on the isolated side of the ADE7933/ADE7932s are not powered and stop working.

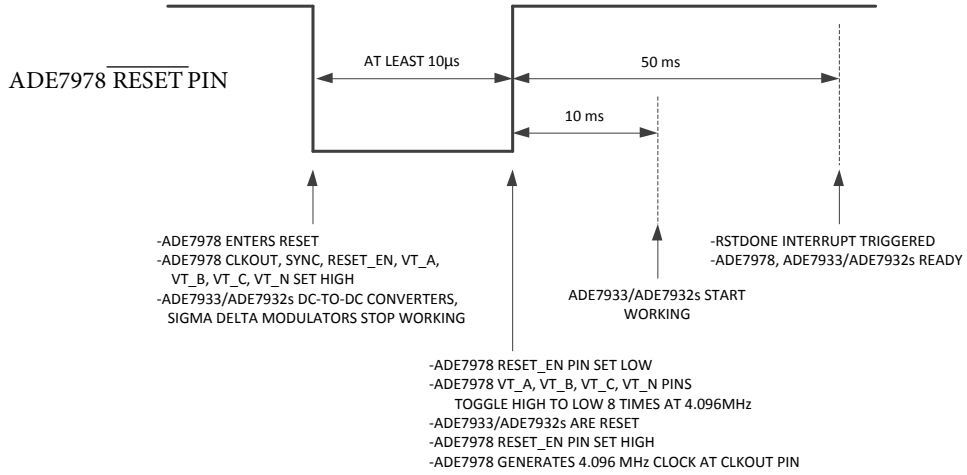


Figure 25. ADE7978/ADE7933/ADE7932 chipset during hardware reset

The ADE7978 generates signals to reset the ADE7933/ADE7932s. When the ADE7978 $\overline{\text{RESET}}$ pin is toggled back high after at least 10 µs, the ADE7978 $\overline{\text{RESET\_EN}}$ pin sets low and the VT_A, VT_B, VT_C and VT_N toggle 8 times high to low with 4.096 MHz frequency (CLKIN/4). This resets the ADE7933/ADE7932s. Then the $\overline{\text{RESET\_EN}}$ pin is set back high and the ADE7978 starts generating a 4.096MHz (CLKIN/4) at CLKOUT pin. This clocks the ADE7933/ADE7932s and they start working.

All the ADE7978 registers are set to their default values. The ADE7978 signals the end of the transition period by triggering the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is 0 during the transition period and becomes 1 when the transition ends. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is returned high by writing to the STATUS1 register with the corresponding bit set to 1. The ADE7978 and the ADE7933/ADE7932s are ready.

After a hardware reset, the DSP is in idle mode, which means it does not execute any instruction.

Because the I²C port is the default serial port of the ADE7978, it becomes active after a reset state. If SPI is the port used by the external microprocessor, the procedure to enable it must be repeated immediately after the $\overline{\text{RESET}}$ pin is toggled back to high (see the Serial Interfaces section for details).

At this point, it is recommended to initialize all of the ADE7978 registers, enable the DSP RAM write protection and then write 0x0001 into the Run register to start the DSP. See the Digital Signal Processor section for details on data memory RAM protection and the Run register.

ADE7978/ADE7933/ADE7932 CHIPSET SOFTWARE RESET FUNCTIONALITY

Bit 7 (SWRST) in the CONFIG register manages the software reset functionality of the ADE7978 and the ADE7933/ADE7932s. The default value of this bit is 0. If this bit is set to 1, then the ADE7978 and the ADE7933/ADE7932s enter the software reset state. In this state, all internal registers are set to their default values. In addition, the choice of which serial port, I²C or SPI, is in use remains unchanged if the lock-in procedure has been executed previously (see the Serial Interfaces section for details). The bit 0 (I2C_LOCK) in CONFIG2 register, if set to 1, locks the selected serial port and it is not changed by a software reset.

When the software reset ends, Bit 7 (SWRST) in the CONFIG register is cleared to 0, the $\overline{\text{IRQ1}}$ interrupt pin is set low, and Bit 15 (RSTDONE) in the STATUS1 register is set to 1. This bit is 0 during the transition period and becomes 1 when the transition ends. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set back high by writing to the STATUS1 register with the corresponding bit set to 1.

After a software reset ends, the DSP is in idle mode, which means it does not execute any instruction. As a good programming practice, it is recommended to initialize all the ADE7978 registers , enable the DSP RAM write protection and then write 0x0001 into the Run register to start the DSP (see the Digital Signal Processor section for details on data memory RAM protection and for details on the Run register).

During the software reset, the ADE7978 also resets the ADE7933/ADE7932s. While CLKOUT signal is still generated at CLKOUT pin, it sets the $\overline{\text{RESET\_EN}}$ pin low and then toggles high to low 8 times at 4.096 MHz (CLKIN/4) the VT_A, VT_B, VT_C and VT_N pins. Then, the $\overline{\text{RESET\_EN}}$, VT_A, VT_B, VT_C and VT_N pins are set back high and the reset ends.

ADE7933/ADE7932 SOFTWARE RESET FUNCTIONALITY

If it is desired to reset only the ADE7933/ADE7932s while maintaining ADE7978 functional, bits 6 (CLKOUT_DIS) and 7 (ADE7933_SWRST) in CONFIG3 register accommodate it. The CLKOUT_DIS bit disables the clock to the ADE7933/ADE7932s by setting the ADE7978 CLKOUT pin high. The ADE7933_SWRST bit resets the ADE7933/ADE7932s by setting the $\overline{\text{RESET\_EN}}$ pin low and toggling high to low 8 times at 4.096 MHz (CLKIN/4) the VT_A, VT_B, VT_C and VT_N pins. When the reset ends, the ADE7933_SWRST bit is cleared to 0.

The recommended procedure to software rest the ADE7933/ADE7932s is:

-write CONFIG3 register with bits 6 (CLKOUT_DIS) and 7 (ADE7933_SWRST) set to 1.

-read back CONFIG3 register until bit 7 (ADE7933_SWRST) is read 0, signaling the reset has ended.

-write CONFIG3 register with bit 6 (CLKOUT_DIS) cleared to 0 to generate clock to the ADE7933/ADE7932.

POWER DOWN MODE

There are situations in which the ADE7978 and ADE7933/ADE7932 chipset does not need to function and it is desirable to lower the current consumption of the chipset. It is recommended to proceed as follows:

-software reset the ADE7933/ADE7932s: write CONFIG3 register with bits (CLKOUT_DIS) and 7 (ADE7933_SWRST) set to 1.

-pull $\overline{\text{RESET}}$ pin low and keep it in this state as long as the power down mode is desired.

THEORY OF OPERATION

ADE7933/ADE7932 ANALOG INPUTS

The ADE7933 has three analog inputs, one current and two voltage channels. The ADE7932 does not include the second voltage channel. The current channel has two fully differential voltage input pins: IP and IM that accept a maximum differential signal of ±31.25 mV.

The maximum signal level on analog inputs for the IP/IM with respect to GND_{ISO} is also ±31.25 mV. The maximum common-mode signal allowed on the inputs is ±25 mV. Figure 26 presents a schematic of the input for the current channels and their relation to the maximum common-mode voltage.

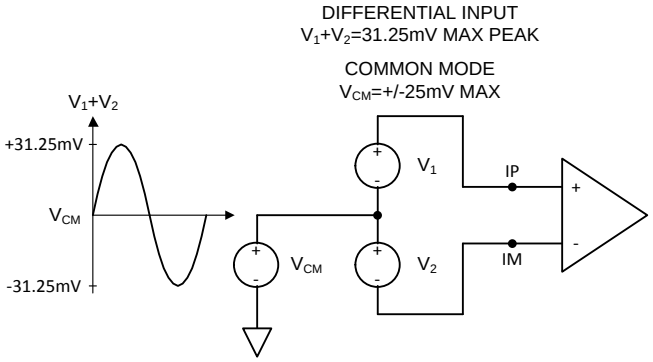


Figure 26. Maximum Input Level, Current Channel

The voltage channels have two pseudo differential, single-ended voltage input pins: V1P and V2P. These single ended voltage inputs have a maximum input voltage of ±0.5 V with respect to VM. The maximum signal level on analog inputs for VxP and VM is also ±0.5 V with respect to GND_{ISO}. The maximum common-mode signal allowed on the inputs is ±25mV. Figure 27 presents a schematic of the voltage channels inputs and their relation to the maximum common-mode voltage.

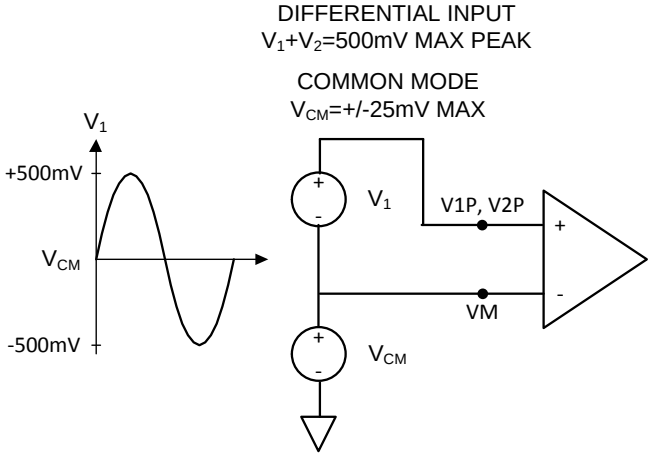


Figure 27. Maximum Input Level, Voltage Channels

ANALOG-TO-DIGITAL CONVERSION

The ADE7933/ADE7932 has three sigma-delta (Σ-Δ) analog-to-digital converters (ADCs). For simplicity, the block diagram in Figure 28 shows a first-order Σ-Δ ADC. The converter is composed of the Σ-Δ modulator and the digital low-pass filter, separated by the digital isolation block.

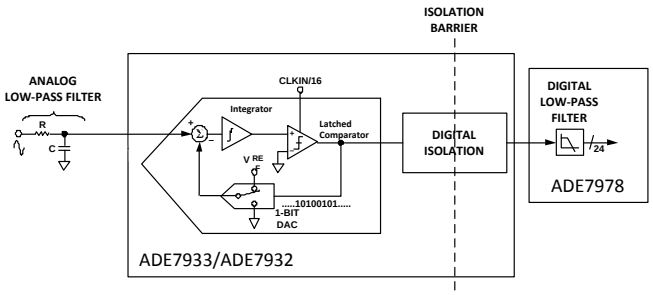


Figure 28. First-Order Σ-Δ ADC

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7933/ADE7932, the sampling clock is equal to 1.024 MHz (CLKIN/16). The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and, therefore, the bit stream) can approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged is a meaningful result obtained. This averaging is carried out in the second part of the ADC, the digital low-pass filter, after the data passed through the digital isolators. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is oversampling. Oversampling means that the signal is sampled at a rate (frequency) that is many times higher than the bandwidth of interest. For example, when CLKIN=4.096 MHz, the sampling rate in the ADE7933/ADE7932 is 1.024 MHz, while the bandwidth of interest is 40 Hz to 3.3 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered, as shown in Figure 29. However, oversampling alone is not efficient enough to improve the signal-to-noise ratio (SNR) in the band of interest. For example, an oversampling factor of 4 is required just to increase the SNR by a mere 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass-type response for the quantization noise. This is the second technique used to achieve high resolution. The result is that most of the noise is at the higher frequencies where it can be removed by the digital low-pass filter present in the ADE7978. This noise shaping is shown in Figure 29.

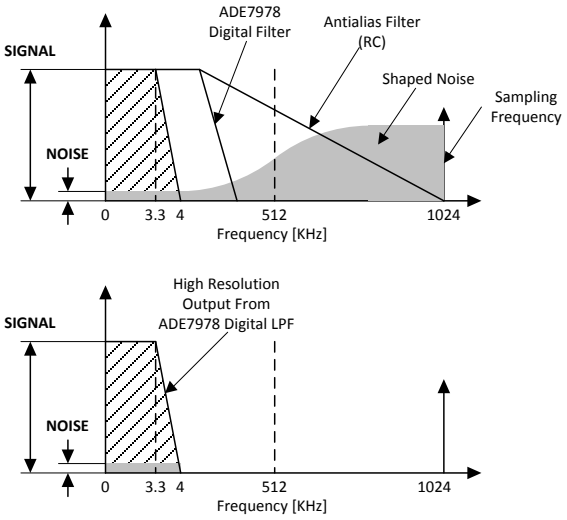


Figure 29. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

Antialiasing Filter

Figure 28 also shows an analog low-pass filter (RC) on the input to the ADC. This filter is placed outside the ADE7933/ADE7932, and its role is to prevent aliasing. Aliasing is an artifact of all sampled systems as shown in Figure 30. Aliasing means that frequency components in the input signal to the ADC, which are higher than half the sampling rate of the ADC, appear in the sampled signal at a frequency below half the sampling rate. Frequency components above half the sampling frequency (also known as the Nyquist frequency, that is, 512 kHz) are imaged or folded back down below 512 kHz. This happens with all ADCs regardless of the architecture. In the example shown, only frequencies near the sampling frequency, that is, 1.024 MHz, move into the band of interest for metering, that is, 40 Hz to 3.3 kHz. To attenuate the high frequency (near 1.024 MHz) noise and prevent the distortion of the band of interest, a low-pass filter (LPF) must be introduced. It is recommended to use one RC filter with a corner frequency of 5 kHz for the attenuation to be sufficiently high at the sampling frequency of 1.024 MHz. The 20 dB per decade attenuation of this filter is usually sufficient to eliminate the effects of aliasing for conventional current sensors.

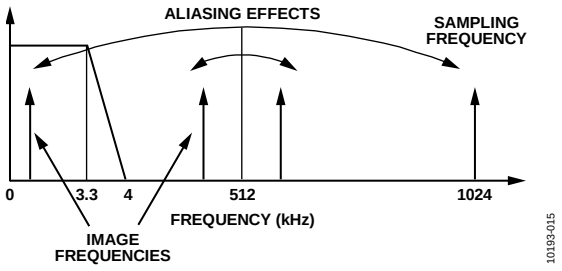


Figure 30. Aliasing Effects

ADC Transfer Function

The ADE7933/ADE7932 provides a stream of bits at DATA pin based on SYNC clock signal provided by the ADE7978 (see Bit-Stream Communication between ADE7978 and ADE7933 section for details). The ADE7978 digital filter elaborates the bit streams coming from all ADE7933/ADE7932s of the system and produces the 24-bit signed output codes of the ADCs.

With a full-scale input signal of 31.25 mV on the current channel, 0.5 V on the voltage channels and an internal reference of 1.2 V, the ADC output code is nominally 5,320,000 and usually varies for each ADE7933/ADE7932 around this value. The ADE7978 obtained code from the ADE7933/ADE7932 ADCs can vary between 0x800000 (−8,388,608) and 0x7FFFFF (+8,388,607); this is equivalent to an input signal level of ±49.27 mV on the current channel and ±0.788 V on the voltage channels. However, for specified performance, do not exceed the nominal range of ±31.25 mV for the current channel and ±0.5 V for the voltage channels; ADC performance is guaranteed only for input signals within these limits.

CURRENT CHANNEL ADC

In the following, the measurements obtained on the current channel of the ADE7933/ADE7932s monitoring the phases A, B and C are called IA, IB and respectively IC (See Figure 14). The measurement obtained on the current channel of the ADE7933/ADE7932 monitoring the neutral current is called IN (See Figure 15).

Figure 31 shows the signal processing path for Input IA (it is the same for IB and IC). The ADC outputs are signed twos complement 24-bit data-words and are available at a rate of 8 kSPS (thousand samples per second). With the specified full-scale analog input signal of ±31.25 mV, the ADC produces its maximum output code value. Figure 31 shows a full-scale voltage signal applied to the differential inputs (IP and IM). The ADC output swings between -5,320,000 and +5,320,000. Note that these are nominal values and every ADE7978 and ADE7933/ADE7932 chipset varies around these values. The input IN, corresponds to the neutral current of a 3-phase system. If the neutral line is not monitored, connect the DATA_N pin of the ADE7978 to VDD. The datapath of the neutral current is similar to the path of the phase currents as shown in Figure 32.

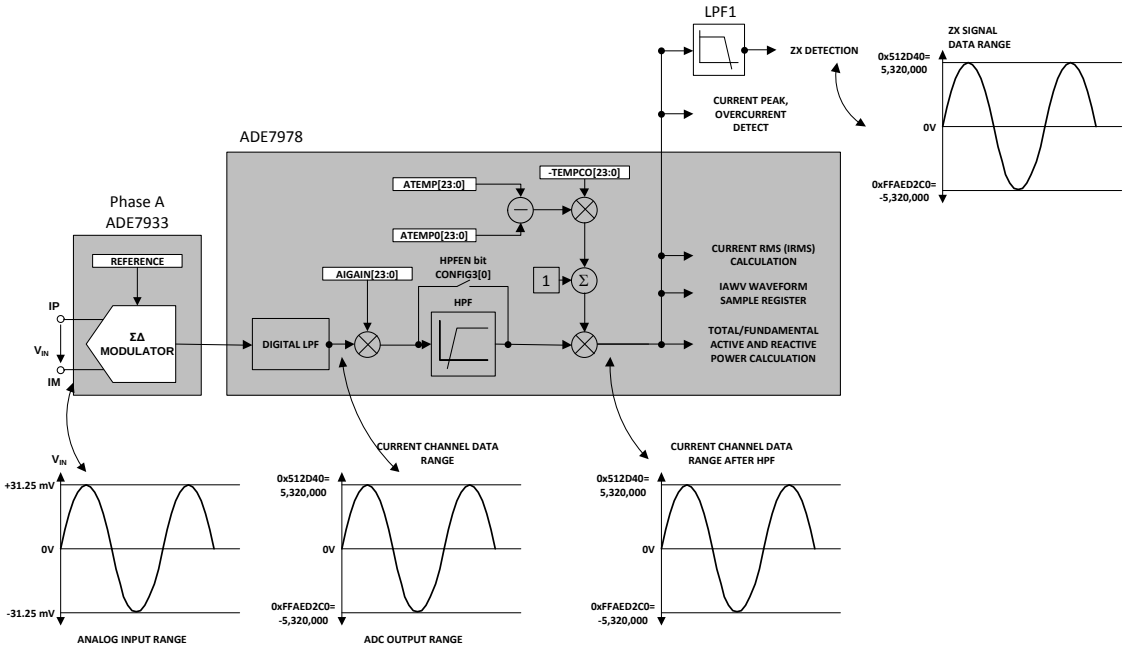


Figure 31. Current Channel Signal Path

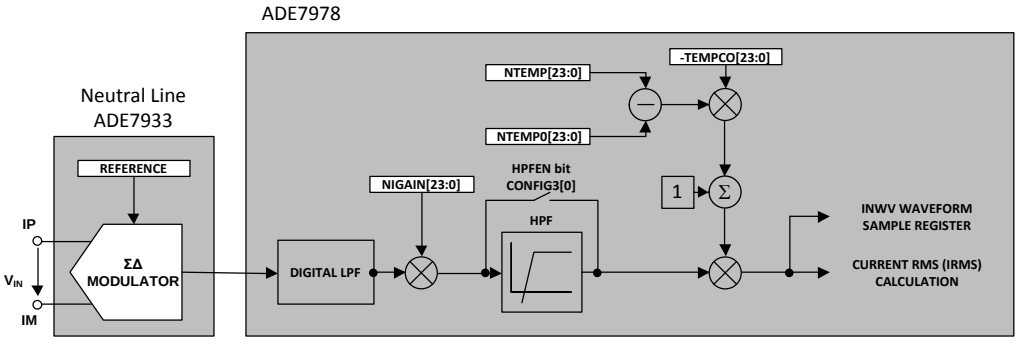


Figure 32. Neutral Current Signal Path

Current Waveform Gain Registers

There is a multiplier in the signal path of each phase and neutral current. The current waveform can be changed by ±100% by writing a corresponding twos complement number to the 24-bit signed current waveform gain registers (AIGAIN, BIGAIN, CIGAIN, and NIGAIN). For example, if 0x400000 is written to those registers, the ADC output is scaled up by 50%. To scale the input by −50%, write 0xC00000 to the registers. Equation (6) describes mathematically the function of the current waveform gain registers.

Current Waveform =

$$ADC\,Output \times \left(1 + \frac{Content\ of\ Current\ Gain\ Register}{2^{23}}\right) \qquad (6)$$

Changing the content of the AIGAIN, BIGAIN, CIGAIN, or NIGAIN registers affects all calculations based on its current; that is, it affects the corresponding phase active/reactive/ apparent energy and current rms calculation. In addition, waveform samples scale accordingly.

Note that the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words, and the DSP works on 28 bits. The 24-bit AIGAIN, BIGAIN, CIGAIN, and NIGAIN registers are accessed as 32-bit registers with the four most significant bits (MSBs) padded with 0s and sign extended to 28 bits. See Figure 33 for details.

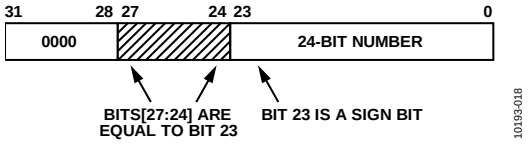


Figure 33. 24-Bit xIGAIN Transmitted as 32-Bit Words

The ADE7933/ADE7932 contains a temperature sensor internally multiplexed with the second voltage measurement V2P (see 2nd Voltage Channel and Temperature Measurement section for more details on the temperature measurement). The ADE7978 assumes all the shunts used in the system have the

same temperature coefficient. The 24-bit signed register TEMPCO contains the negative value of the temperature coefficient.

Assume the shunt resistance R varies linearly according to the formula:

$$R = R_0 \times \left[1 + \varepsilon \times \left(T - T_0\right)\right] \quad (7)$$

Where:

R_0 is the shunt resistance at nominal temperature T_0.

ε is the shunt's temperature coefficient.

T is the temperature of the shunt.

To compensate for this resistance increase, the current waveform must be divided by $1+\varepsilon \times (T-T_0)$. Because ε is a very small number, this is equivalent to a multiplication by $1-\varepsilon \times (T-T_0)$:

$$\text{Current waveform} = \text{ADC Output} \times \left[1 - \varepsilon \times \left(T - T_0\right)\right] \quad (8)$$

A multiplier has been introduced in the data path signal path of each phase and neutral current. The 24-bit signed register TEMPCO stores the shunt's temperature coefficient ε taken with negative sign. Because the ADE7978 measures the temperature of each ADE7933/ADE7932 and stores it into ATEMP, BTEMP, CTEMP, and NTEMP registers in 10^{-1} °C units, TEMPCO must be initialized as the signed 24-bit fixed-point number equal to $-10^{-1} \times \varepsilon$. For example, if ε=50ppm/°C:

$\text{TEMPCO} = \text{round}(2^{24} - 10^{-1} \times 50 \times 10^{-6} \times 2^{23}) = 0\text{xFFFFD6}$.

The 24-bit signed registers ATEMP0, BTEMP0, CTEMP0 and NTEMP0 represent the ambient temperature T_0 (in 10^{-1} °C units) at which the meter temperature sensor gain calibration has been executed on every phase (see 2nd Voltage Channel and Temperature Measurement section). The 24-bit signed registers ATEMP, BTEMP, CTEMP and NTEMP represent the shunt temperatures T (in 10^{-1} °C units) measured by the temperature sensor of every ADE7933/ADE7932 of the system. The temperature sensor measurement starts when the VT_A, VT_B, VT_C and VT_N pins are set low and the results are first stored into ATEMP, BTEMP, CTEMP, and NTEMP registers 1.024s after (see 2nd Voltage Channel and Temperature Measurement section). Only then, the temperature compensation scheme becomes active and works at an 8kHz update rate.

The Expression (9) describes mathematically the function of the current waveform temperature compensation:

$$\text{Current Waveform} = \text{=ADC Output} \times \left[1 + \text{TEMPCO} \times (\text{TEMP} - \text{TEMP0})\right] \quad (9)$$

Current Channel HPF

The ADC outputs can contain a dc offset. This offset can create errors in power and rms calculations. High-pass filters (HPFs) are placed in the signal path of the phase and neutral currents and of the phase voltages. If enabled, the HPF eliminates any dc offset on the current channel. All filters in both current and voltage channels are implemented in the DSP and, by default, they are all enabled: Bit 4 (HPFEN) of the CONFIG[15:0] register is set to 1. All filters are disabled by setting Bit 0 (HPFEN) to 0.

Current Channel Sampling

The waveform samples of the current channel are taken at the output of HPF and stored in the 24-bit signed registers, IAWV, IBWV, ICWV, and INWV at a rate of 8 kSPS. All power and rms calculations remain uninterrupted during this process. Bit 17 (DREADY) in the STATUS0 register is set when the IAWV, IBWV, ICWV, and INWV registers are available to be read using the I^2C or SPI serial port. Setting Bit 17 (DREADY) in the MASK0 register enables an interrupt to be set when the DREADY flag is set. See the Digital Signal Processor section for more details on Bit DREADY. Additionally, if bits 1, 0 (ZX_DREADY) in CONFIG register are set to 00, $\overline{\text{DREADY}}$ functionality is selected at ZX/$\overline{\text{DREADY}}$ pin. In this case, the pin goes low 6.5µs before bit DREADY is set to 1 in the STATUS0 register. It stays low for 10µs and then goes back high. Use $\overline{\text{DREADY}}$ pin low to high transition to initiate a burst read of the waveform sample registers. See I^2C Burst Read Operation and SPI Burst Read Operation sections for details. For the ZX functionality at ZX/$\overline{\text{DREADY}}$ pin, that is when bits ZX_DREADY are set to 01, 10 or 11, see Zero-Crossing Detection section.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words. When the IAWV, IBWV, ICWV, and INWV 24-bit signed registers are read from theADE7978, they are transmitted sign extended to 32 bits. See Figure 34 for details.

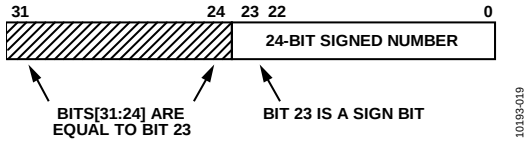


Figure 34. 24-Bit IxWV Register Transmitted as 32-Bit Signed Word

The ADE7978 contains a high speed data capture (HSDC) port that is specially designed to provide fast access to the waveform sample registers. See the HSDC Interface section for more details.

VOLTAGE CHANNEL ADCS

In the following, the measurements obtained on the ADE7933/ADE7932s voltage channels monitoring the phases A, B and C are called VA, VB and respectively VC (See Figure 14). The measurement obtained on the voltage channel of the ADE7933/ADE7932 monitoring the neutral to earth voltage is called VN (See Figure 15). They represent the signals measured between V1P and VM pins of the ADE7933/ADE7932s of the system. The signals measured between V2P and VM pins of the ADE7933/ADE7932s are called VA2, VB2, VC2 and VN2.

Figure 35 shows the ADC and signal processing chain for Input VA in the voltage channel. The VB and VC channels have similar processing chains. The ADC outputs are signed twos complement 24-bit words and are available at a rate of 8 kSPS.

With the specified full-scale analog input signal of ±0.5 V, the ADC produces its maximum output code value. Figure 35 shows a full-scale voltage signal being applied to the differential inputs (V1P and VM). The ADC output swings between -5,320,000 and +5,320,000. Note these are nominal values and every ADE7978/ADE7933/ADE7932 chipset varies around these values. The input VN between V1P and VM pins of the neutral line ADE7933/ADE7932 corresponds to the earth to neutral voltage of a 3-phase system. If no voltage is monitored at V1P pin, connect V1P pin to VM pin. The datapath of the earth to neutral voltage is similar to the path of the phase voltages as shown in Figure 36.

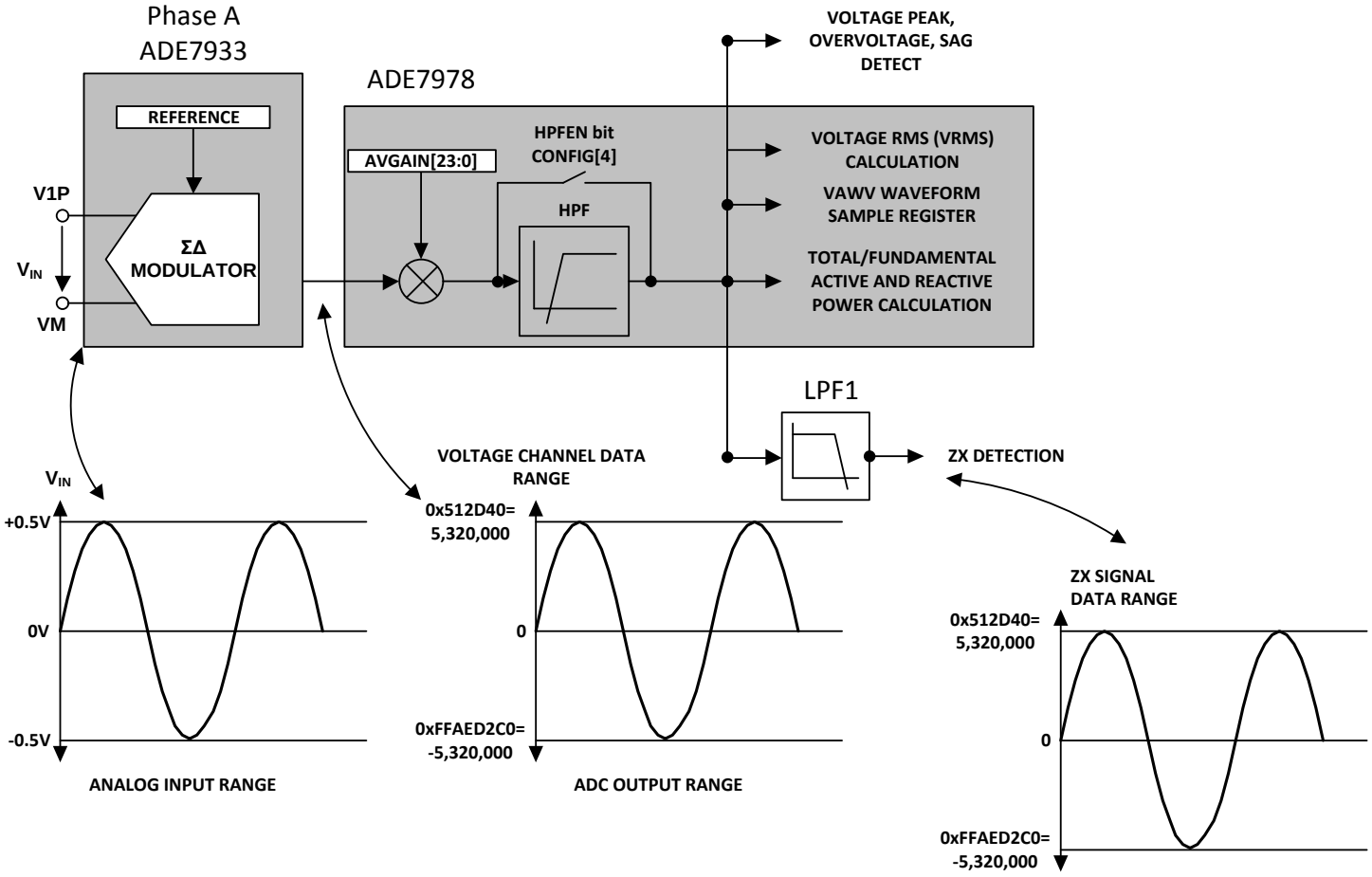


Figure 35. Phase A to Neutral Voltage Channel Datapath

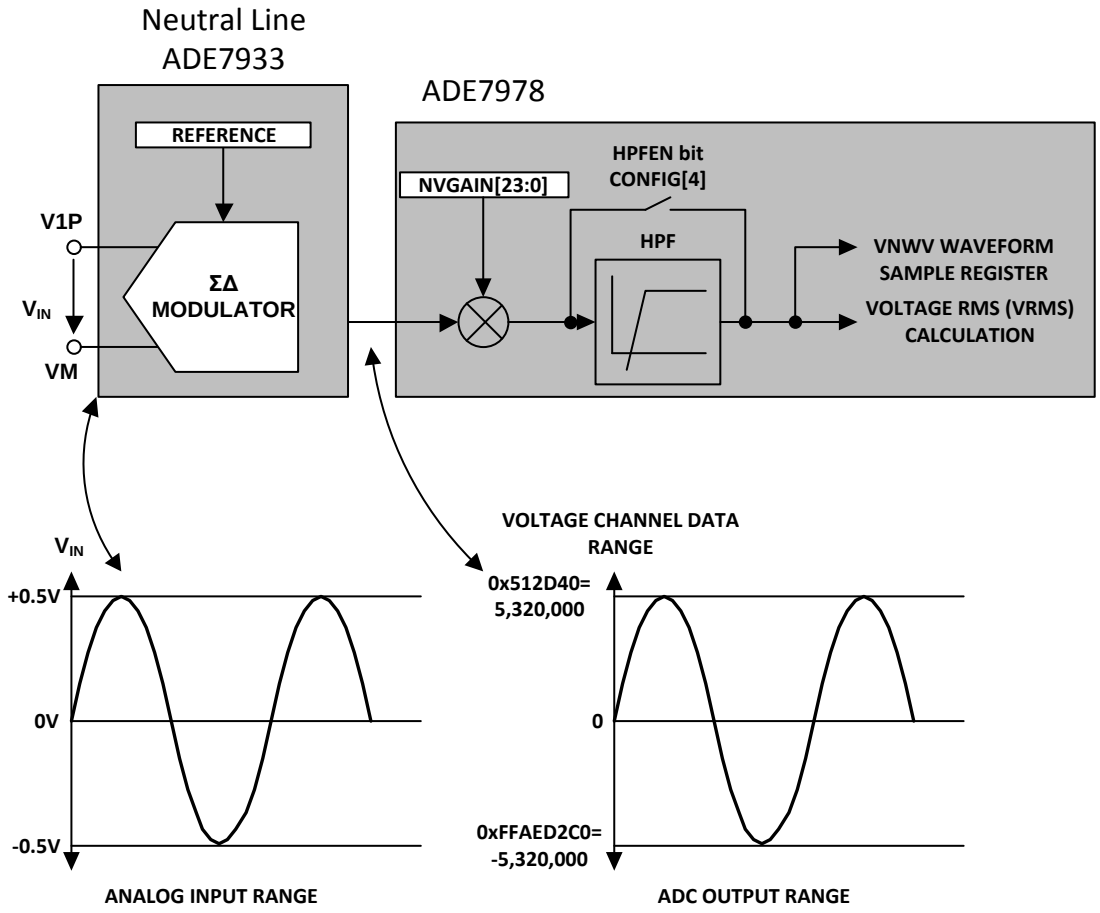


Figure 36. Earth to Neutral Voltage Channel Datapath

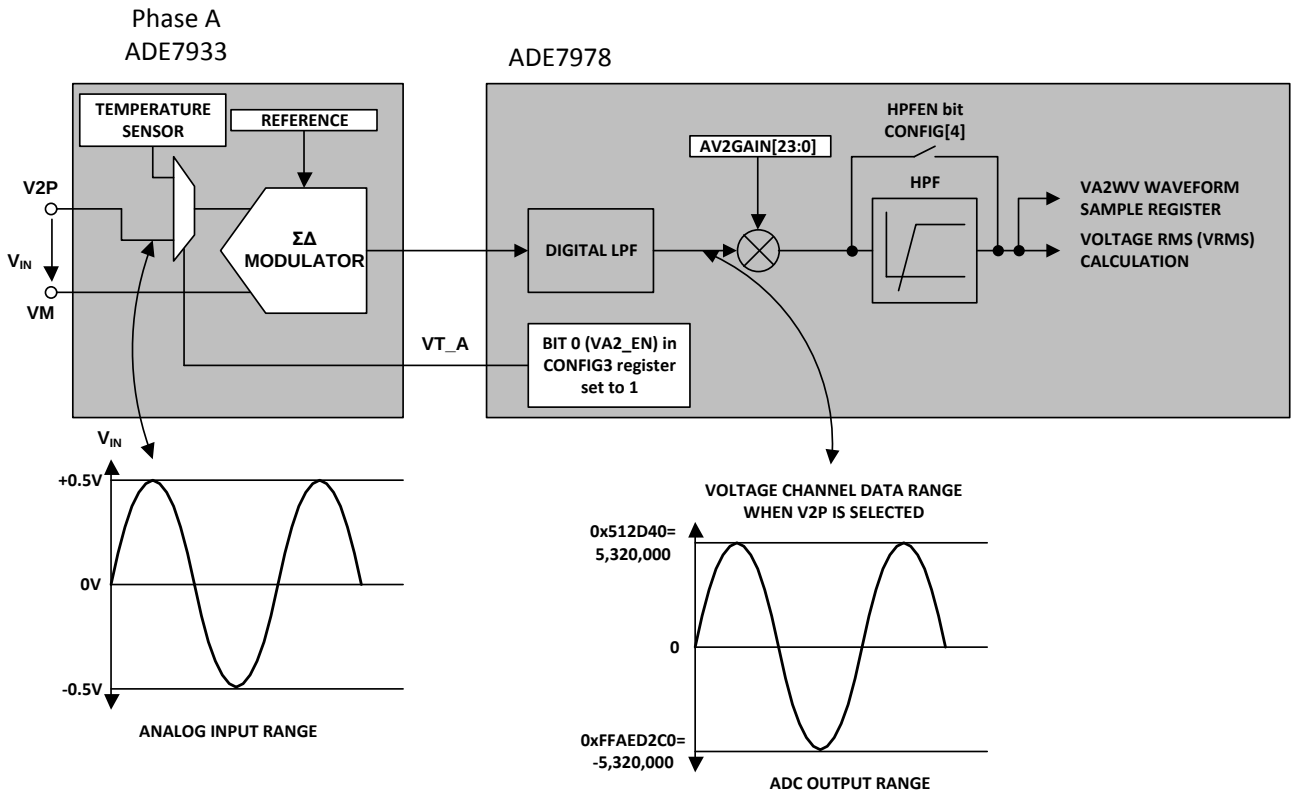


Figure 37. Phase A V2P Channel Datapath (ADE7933 only)

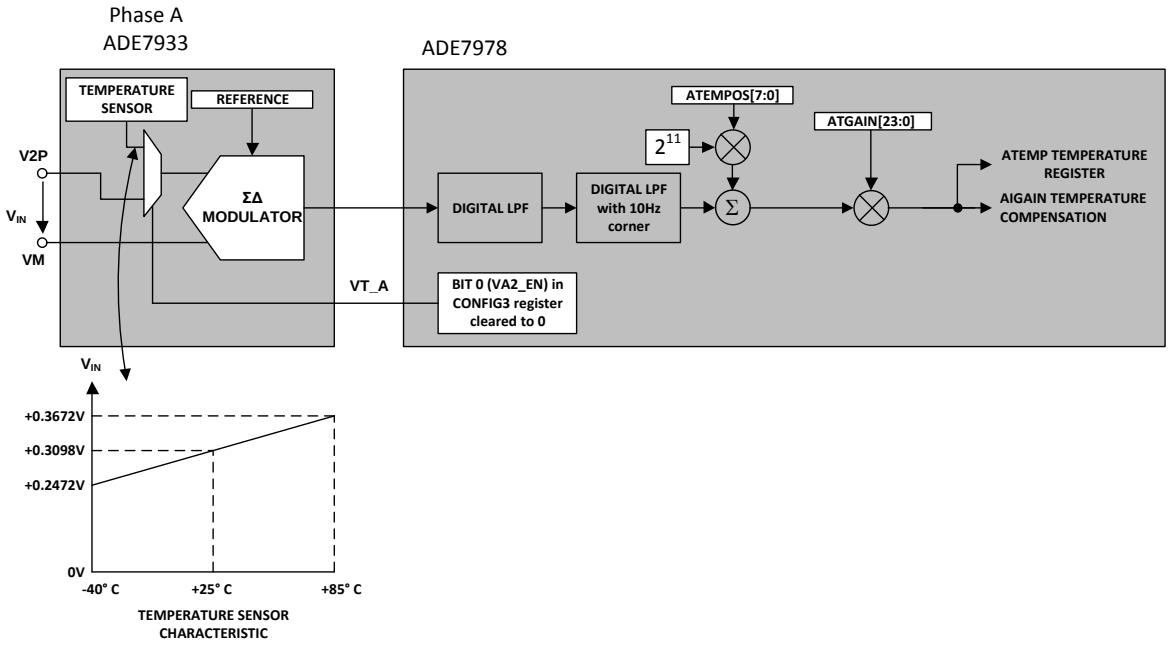


Figure 38. Temperature Measurement Datapath

2nd Voltage Channel and Temperature Measurement

Figure 37 presents the ADC and signal processing chain for the input VA2 in the voltage channel (ADE7933 only). The input V2P pin of the ADE7933/ADE7932 is multiplexed with a temperature sensor. On the ADE7932, the VA2 channel is not available and the V2P pin must be connected to VM. If no voltage is monitored at V2P pin, connect V2P to VM pin. The VB2, VC2 and VN2 channels have similar processing chains.

On the ADE7933/ADE7932, the selection is done based on the state of the V2/$\overline{\text{TEMP}}$ pin. Connect the V2/$\overline{\text{TEMP}}$ pin of the ADE7933/ADE7932 monitoring the phases A, B and C to VT_A, VT_B and VT_C pins of the ADE7978 (See Figure 1). Connect the V2/$\overline{\text{TEMP}}$ pin of the ADE7933/ADE7932 monitoring the neutral line to VT_N pin of the ADE7978.

The V2/$\overline{\text{TEMP}}$ pin is also used during the reset procedure of the ADE7933/ADE7932 (see Hardware Reset section).

On the ADE7978, the selection is done based on bits 0, 1, 2 and 3 (VA2_EN, VB2_EN, VC2_EN and VN2_EN) in CONFIG3 register. When the bits are set to 1, the default value, the VT_A, VT_B, VT_C and VT_N pins are set high and VA2, VB2, VC2 and VN2 are measured. When the bits are cleared to 0, the VT_A, VT_B, VT_C and VT_N pins are set low and the temperature sensors of each ADE7933/ADE7932 are measured.

Figure 38 presents the ADC and signal processing chain for the temperature sensor when the ADE7933/ADE7932 monitors the phase A. The temperature measurement is characterized by offset and gain errors. The offset information is calculated during the manufacturing process and it is stored with opposite sign into the ADE7933/ADE7932. The ADE7978 reads it using the bit stream communication (see Bit-Stream Communication between ADE7978 and ADE7933 section for more details).

Then it stores it into ATEMPOS, BTEMPOS, CTEMPOS, NTEMPOS 8-bit signed registers. The offset information is shifted left by 11 bits before being added to the temperature data path.

The gain compensation uses ATGAIN, BTGAIN, CTGAIN and NTGAIN 24-bit signed temperature gain registers that change the temperature waveform by ±100%. For example, if 0x400000 is written to those registers, the ADC output is scaled up by 50%. To scale the input by –50%, write 0xC00000 to the registers. Equation 10 describes mathematically the function of the current waveform gain registers.

Temperature Waveform =

$$ADC\ Output \times \left(1 + \frac{Content\ of\ Temp\ Gain\ Register}{2^{23}}\right) \quad (10)$$

For a temperature measurement maximum accuracy of ±5°C across the -40°C to +85°C operating temperature range and a result expressed in 10^{-1} °C units, the gain registers ATGAIN, BTGAIN, CTGAIN and NTGAIN should be setup equal to 0x8121E5, the signed 24-bit representation of 8.846915×10^{-4}-1.

Instead of using the default value, the gain registers ATGAIN, BTGAIN, CTGAIN and NTGAIN may be calibrated as part of the overall meter calibration process. Just measure the temperature of every ADE7933/ADE7932, set accordingly the ATEMP0, BTEMP0, CTEMP0 and NTEMP0 registers in 10^{-1} °C units, read V2WV register containing the temperature sensor reading of every ADE7933/ADE7932 and compute the gains as follows:

$$xTGAIN = \frac{xTEMP0}{xTEMP} - 1 \quad (11)$$

The temperature measurement results are stored into the ATEMP, BTEMP, CTEMP and NTEMP 24-bit signed registers 1.024s after the temperature sensor measurement was started by setting low VT_A, VT_B, VT_C and VT_N pins. Then they are updated at 8kSPS rate. Keep the VT_A, VT_B, VT_C and VT_N pins low at least 1.024s in order for the temperature measurement results to be stored into the ATEMP, BTEMP, CTEMP and NTEMP registers. To obtain the final temperature measurement expressed in 10^{-1} °C units, the microcontroller has to subtract 3200 from xTEMP registers.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words. Similar to registers presented in Figure 47, the ATEMP, BTEMP, CTEMP and NTEMP 24-bit signed registers are transmitted with the eight MSBs padded with 0s.

Voltage Waveform Gain Registers

There is a multiplier in the signal path of each phase voltage. The voltage waveform can be changed by ±100% by writing a corresponding twos complement number to the 24-bit signed voltage waveform gain registers (AVGAIN, AV2GAIN, BVGAIN, BV2GAIN, CVGAIN, CV2GAIN, NVGAIN and NV2GAIN). For example, if 0x400000 is written to those registers, the ADC output is scaled up by 50%. To scale the input by –50%, write 0xC00000 to the registers. Equation (12) describes mathematically the function of the current waveform gain registers.

$$Voltage\ Waveform = ADC\ Output \times \left(1 + \frac{Content\ of\ Voltage\ Gain\ Register}{2^{23}}\right) \quad (12)$$

Changing the content of the AVGAIN, AV2GAIN, BVGAIN, BV2GAIN, CVGAIN, CV2GAIN, NVGAIN and NV2GAIN registers affects all calculations based on its voltage; that is, it affects the corresponding phase active/reactive/apparent energy and voltage rms calculation. In addition, waveform samples are scaled accordingly.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words, and the DSP works on 28 bits. As presented in Figure 33, the AVGAIN, AV2GAIN, BVGAIN, BV2GAIN, CVGAIN, CV2GAIN, NVGAIN and NV2GAIN registers are accessed as 32-bit registers with four MSBs padded with 0s and sign extended to 28 bits.

Voltage Channel HPF

As explained in the Current Channel HPF section, the ADC outputs can contain a dc offset that can create errors in power and rms calculations. HPFs are placed in the signal path of the phase voltages and in the current channels. Bit 4 (HPFEN) of CONFIG register can enable or disable all the filters in both voltage and current channels. See the Current Channel HPF section for more details.

Voltage Channel Sampling

The waveform samples of the voltage channel are taken at the output of HPF and stored into VAWV, VA2WV, VBWV, VB2WV, VCWV, VC2WV, VNWV, and VN2WV 24-bit signed registers at a rate of 8 kSPS. All power and rms calculations remain uninterrupted during this process. Bit 17 (DREADY) in the STATUS0 register is set when the VAWV, VA2WV, VBWV, VB2WV, VCWV, VC2WV, VNWV, and VN2WV registers are available to be read using the I²C or SPI serial port. Setting Bit 17 (DREADY) in the MASK0 register enables an interrupt to be set when the DREADY flag is set. See the Digital Signal Processor section for more details on Bit DREADY. Additionally, if bits 1, 0 (ZX_DREADY) in CONFIG register are set to 00, $\overline{\text{DREADY}}$ functionality is selected at ZX/$\overline{\text{DREADY}}$ pin. In this case, the pin goes low 6.5µs before bit DREADY is set to 1 in the STATUS0 register. It stays low for 10µs and then goes back high. Use $\overline{\text{DREADY}}$ pin low to high transition to initiate a burst read of the waveform sample registers. See I²C Burst Read Operation and SPI Burst Read Operation sections for details. For the ZX functionality at ZX/$\overline{\text{DREADY}}$ pin, that is when bits ZX_DREADY are set to 01, 10 or 11, see Zero-Crossing Detection section.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words. Similar to registers presented in Figure 34, the VAWV, VA2WV, VBWV, VB2WV, VCWV, VC2WV, VNWV, and VN2WV 24-bit signed registers are transmitted sign extended to 32 bits.

The ADE7978 contains an HSDC port especially designed to provide fast access to the waveform sample registers. See the HSDC Interface section for more details.

CHANGING PHASE VOLTAGE DATA PATH

The ADE7978 can direct one phase voltage input to the computational data path of another phase. For example, Phase A voltage can be introduced in the Phase B computational data path, which means all powers computed by the ADE7978 in Phase B are based on Phase A voltage and Phase B current.

Bits[9:8] (VTOIA[1:0]) of the CONFIG register manage the Phase A voltage measured by the Phase A ADE7933/ADE7932. If VTOIA[1:0] = 00 (default value), the voltage is directed to the Phase A computational data path. If VTOIA[1:0] = 01, the voltage is directed to the Phase B path. If VTOIA[1:0] = 10, the voltage is directed to the Phase C path. If VTOIA[1:0] = 11, the ADE7978 behaves as if VTOIA[1:0] = 00.

Bits[11:10] (VTOIB[1:0]) of the CONFIG register manage the Phase B voltage measured by the Phase B ADE7933/ADE7932. If VTOIB[1:0] = 00 (default value), the voltage is directed to the Phase B computational data path. If VTOIB[1:0] = 01, the voltage is directed to the Phase C path. If VTOIB[1:0] = 10, the voltage is directed to the Phase A path. If VTOIB[1:0] = 11, the ADE7978 behaves as if VTOIB[1:0] = 00.

Bits[13:12] (VTOIC[1:0]) of the CONFIG register manage the Phase C voltage measuredby the Phase C ADE7933/ADE7932. If VTOIC[1:0] = 00 (default value), the voltage is directed to Phase C computational data path, if VTOIC[1:0] = 01, the voltage is directed to the Phase A path. If VTOIC[1:0] = 10, the voltage is directed to the Phase B path. If VTOIC[1:0] = 11, the ADE7978 behaves as if VTOIC[1:0] = 00.

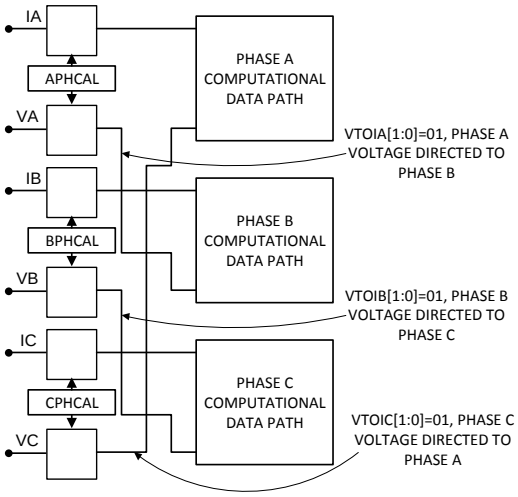


Figure 39. Phase Voltages Used in Different Datapaths

Figure 39 presents the case in which the Phase A voltage is used in the Phase B data path, the Phase B voltage is used in the Phase C data path, and the Phase C voltage is used in the Phase A data path.

POWER QUALITY MEASUREMENTS

Zero-Crossing Detection

The ADE7978 has a zero-crossing (ZX) detection circuit on the phase current and phase voltage channels. The neutral current data path and the second voltage channels do not contain a zero-crossing detection circuit. Zero-crossing events are used as a time base for various power quality measurements and in the calibration process.

The output of LPF1 is used to generate zero crossing events. The low-pass filter is intended to eliminate all harmonics of 50 Hz and 60 Hz systems, and to help identify the zero-crossing events on the fundamental components of both current and voltage channels.

The digital filter has a pole at 80 Hz and is clocked at 256 kHz. As a result, there is a phase lag between the analog input signal (one of IA, IB, IC, VA, VB, and VC) and the output of LPF1. The error in ZX detection is 0.0703° for 50 Hz systems (0.0843° for 60 Hz systems). The phase lag response of LPF1 results in a time delay of approximately 31.4° or 1.74 ms (at 50 Hz) between its input and output. The overall delay between the zero crossing on the analog inputs and ZX detection obtained after LPF1 is about 39.6° or 2.2 ms (at 50 Hz). The ADC and HPF introduce the additional delay. The LPF1 cannot be disabled to assure a good resolution of the ZX detection. Figure 40 shows how the zero-crossing signal is detected.

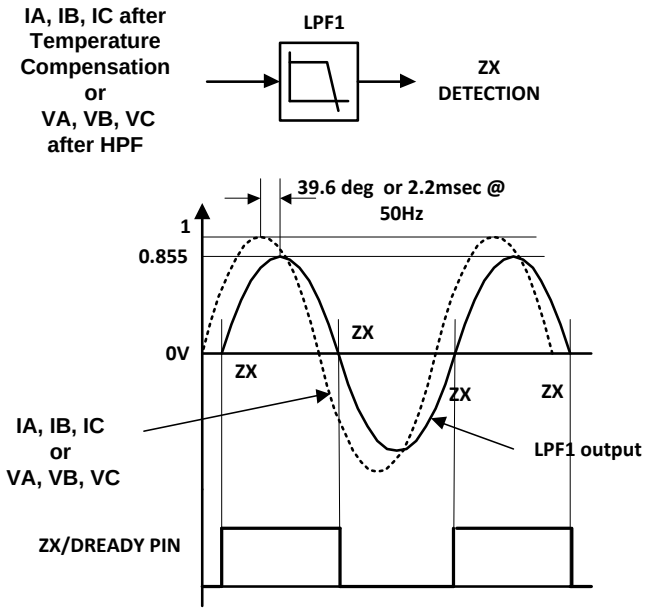


Figure 40. Zero-Crossing Detection on Voltage and Current Channels

To provide further protection from noise, input signals to the voltage channel with amplitude 1000 times lower than full scale do not generate zero-crossing events at all. The Current Channel ZX detection circuit is active for all input signals independent of their amplitudes.

The ADE7978 contains six zero-crossing detection circuits, one for each phase voltage and current channel. Each circuit drives one flag in the STATUS1 register. If a circuit placed in the Phase A voltage channel detects one zero-crossing event, Bit 9 (ZXVA) in the STATUS1 register is set to 1.

Similarly, the Phase B voltage circuit drives Bit 10 (ZXVB), the Phase C voltage circuit drives Bit 11 (ZXVC), and circuits placed in the current channel drive Bit 12 (ZXIA), Bit 13 (ZXIB), and Bit 14 (ZXIC) in the STATUS1 register. If a ZX detection bit is set in the MASK1 register, the $\overline{\text{IRQ1}}$ interrupt pin is driven low and the corresponding status flag is set to 1. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the status bit set to 1.

The ADE7978 provides zero-crossing functionality at ZX/$\overline{\text{DREADY}}$ pin, managed by bits 1,0 (ZX_DREADY) in CONFIG register. When the phase voltage is positive, the ZX pin stays high. When the phase voltage is negative, the ZX pin stays low (Figure 40). When bits ZX_DREADY are 01, the zero crossing events detected on the phase A voltage trigger the ZX/$\overline{\text{DREADY}}$ pin to stay low simultaneously with bit 9 (ZXVA) in STATUS1 being set to 1. When bits ZX_DREADY are 10 and 11, phase B voltage and phase C voltage trigger ZX/$\overline{\text{DREADY}}$ pin functionality simultaneously with bits ZXVB and ZXVC in STATUS1 register being set to 1.

Zero-Crossing Timeout

Every zero-crossing detection circuit has an associated timeout register that starts to decrement 1ms (sixteen cycles of a 16 kHz

clock) after a zero crossing event was triggered . This register is loaded with the value written into the 16-bit ZXTOUT register and is decremented (1 LSB) every 62.5 µs (16 kHz clock). The register is reset to the ZXTOUT value every time a zero crossing is detected. The default value of this register is 0xFFFF. If the timeout register decrements to 0 before a zero crossing is detected, one of Bits[8:3] of the STATUS1 register is set to 1. Bit 3 (ZXTOVA), Bit 4 (ZXTOVB), and Bit 5 (ZXTOVC) in the STATUS1 register refer to Phase A, Phase B, and Phase C of the voltage channel; Bit 6 (ZXTOIA), Bit 7 (ZXTOIB), and Bit 8 (ZXTOIC) in the STATUS1 register refer to Phase A, Phase B, and Phase C of the current channel.

If a ZXTOIx or ZXTOVx bit is set in the MASK1 register, the $\overline{\text{IRQ1}}$ interrupt pin is driven low when the corresponding status bit is set to 1. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is returned to high by writing to the STATUS1 register with the status bit set to 1.

The resolution of the ZXOUT register is 62.5 µs (16 kHz clock) per LSB. Thus, the maximum timeout period for an interrupt is 4.096 sec: 2^{16}/16 kHz. Note that because the timer starts decrementing 1ms after a zero crossing event is triggered, the value of ZXTOUT register is:

$$\text{ZXTOUT}=\text{Desired ZX timeout} \times 16\ \text{kHz}-16 \quad (13)$$

Figure 41 shows the mechanism of the zero-crossing timeout detection when the voltage or the current signal stays at a fixed dc level for more than 62.5 µs × ZXTOUT µs.

When the phase voltage is 0, noise in the voltage measurement may trigger spurious zero crossing events that may nullify the action of the ZX timeout. A threshold 1000 times lower than full scale was implemented in conjunction with this circuit. If the peak of the phase voltage is below this threshold, the ZX timeout counter begins to decrement automatically.

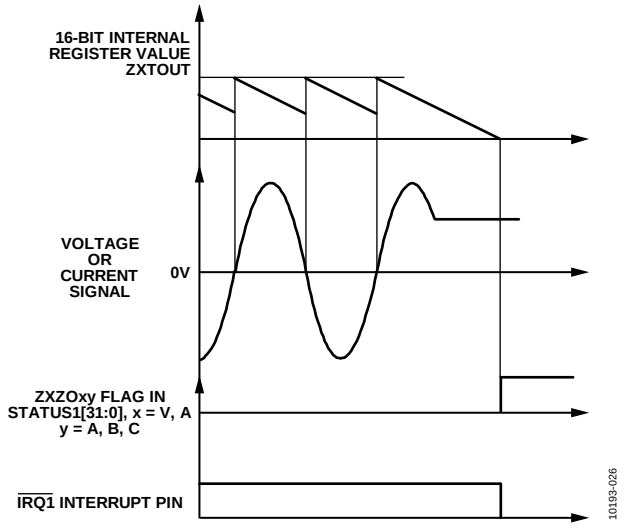


Figure 41. Zero-Crossing Timeout Detection

Phase Sequence Detection

The ADE7978 has on-chip phase sequence error detection circuits. This detection works on phase voltages and considers only the zero crossings determined by their negative-to-positive transitions. The regular succession of these zero-crossing events is Phase A followed by Phase B followed by Phase C (see Figure 43). If the sequence of zero-crossing events is, instead, Phase A followed by Phase C followed by Phase B, then Bit 19 (SEQERR) in the STATUS1 register is set.

If Bit 19 (SEQERR) in the MASK1 register is set to 1 and a phase sequence error event is triggered, the $\overline{\text{IRQ1}}$ interrupt pin is driven low. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set high by writing to the STATUS1 register with the Status Bit 19 (SEQERR) set to 1.

The phase sequence error detection circuit is functional only when the ADE7978/ADE7933/ADE7932 chipset is connected in a 3-phase, 4-wire, three voltage sensors configuration (Bits[5:4], CONSEL[1:0] in the ACCMODE register, set to 00). In all other configurations, only two voltage sensors are used; therefore, it is not recommended to use the detection circuit. In these cases, use the time intervals between phase voltages to analyze the phase sequence (see the Time Interval Between Phases section for details).

Figure 42 presents the case in which Phase A voltage is not followed by Phase B voltage but by Phase C voltage. Every time a negative-to-positive zero crossing occurs, Bit 19 (SEQERR) in the STATUS1 register is set to 1 because such zero crossings on Phase C, Phase B, or Phase A cannot come after zero crossings from Phase A, Phase C, or respectively, Phase B zero crossings.

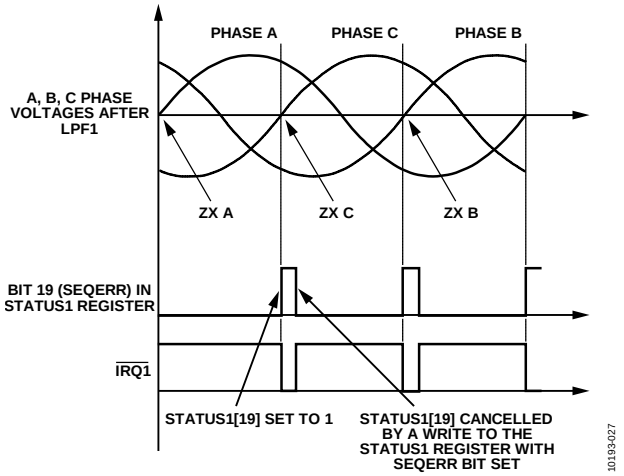


Figure 42. SEQERR Bit Set to 1 When Phase A Voltage Is Followed by Phase C Voltage

Once a phase sequence error has been detected, the time measurement between various phase voltages (see the Time Interval Between Phases section) can help to identify which phase voltage should be considered with another phase current in the computational data path. Bits[9:8] (VTOIA[1:0]), Bits[11:10] (VTOIB[1:0]), and Bits[13:12] (VTOIC[1:0]) in the CONFIG register can be used to direct one phase voltage to the

data path of another phase. See the Changing Phase Voltage Data path section for details.

Time Interval Between Phases

The ADE7978 has the capability to measure the time delay between the phase voltages, between phase currents, or between voltages and currents of the same phase. The negative-to-positive transitions identified by the zero-crossing detection circuit are used as start and stop measuring points. As the zero-crossing events are identified based on the fundamental components of the phase currents and voltages, the time interval measurements relate to the fundamental components. Only one set of such measurements is available at one time, based on Bits[10:9] (ANGLESEL[1:0]) in the COMPMODE register.

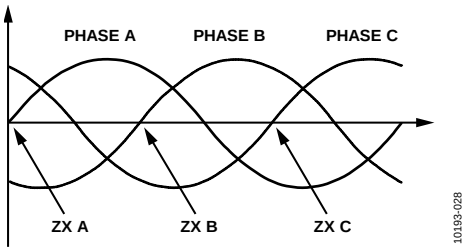


Figure 43. Regular Succession of Phase A, Phase B, and Phase C

When the ANGLESEL[1:0] bits are set to 00, the default value, the delays between voltages and currents on the same phase are measured. The delay between Phase A voltage and Phase A current is stored in the 16-bit unsigned ANGLE0 register (see Figure 44 for details). In a similar way, the delays between voltages and currents on Phase B and Phase C are stored in the ANGLE1 and ANGLE2 registers, respectively.

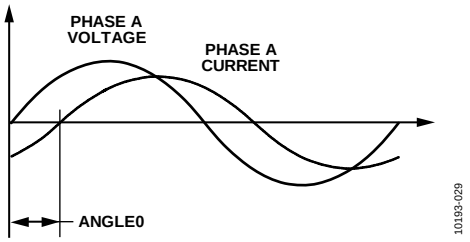


Figure 44. Delay Between Phase A Voltage and Phase A Current Is Stored in the ANGLE0 Register

When the ANGLESEL[1:0] bits are set to 01, the delays between phase voltages are measured. The delay between Phase A voltage and Phase C voltage is stored into the ANGLE0 register. The delay between Phase B voltage and Phase C voltage is stored in the ANGLE1 register, and the delay between Phase A voltage and Phase B voltage is stored in the ANGLE2 register (see Figure 45 for details).

When the ANGLESEL[1:0] bits are set to 10, the delays between phase currents are measured. Similar to delays between phase voltages, the delay between Phase A and Phase C currents is stored into the ANGLE0 register, the delay between Phase B and Phase C currents is stored in the ANGLE1 register, and the delay between Phase A and Phase B currents is stored into the ANGLE2 register (see Figure 45 for details).

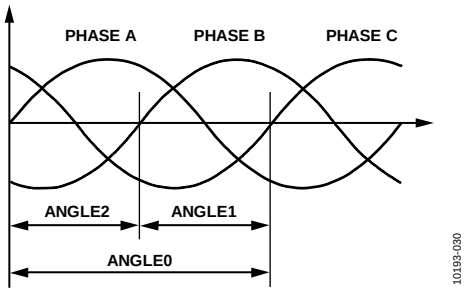


Figure 45. Delays Between Phase Voltages (Currents)

The ANGLE0, ANGLE1, and ANGLE2 registers are 16-bit unsigned registers with 1 LSB corresponding to 3.90625 µs (256 kHz clock), which means a resolution of 0.0703° (360° × 50 Hz/256 kHz) for 50 Hz systems and 0.0843° (360° × 60 Hz/256 kHz) for 60 Hz systems. The delays between phase voltages or phase currents are used to characterize how balanced the load is. The delays between phase voltages and currents are used to compute the fundamental power factor on each phase as shown in the following Equation (14):

$$\cos\varphi_x = \cos\left[ANGLEx \times \frac{360^\circ \times f_{LINE}}{256\,\text{kHz}} \right] \quad (14)$$

where f_{LINE} the line frequency.

Period Measurement

The ADE7978 provides the period measurement of the line in the voltage channel. The period of each phase voltage is measured and stored in three different registers, APERIOD, BPERIOD, and CPERIOD. The period registers are 16-bit unsigned registers and update every line period. Because of the LPF1 filter (see Figure 40), a settling time of 30 ms to 40 ms is associated with this filter before the measurement is stable.

The period measurement has a resolution of 3.90625 µs/LSB (256 kHz clock), which represents 0.0195% (50 Hz/256 kHz) when the line frequency is 50 Hz and 0.0234% (60 Hz/256 kHz) when the line frequency is 60 Hz. The value of the period registers for 50 Hz networks is approximately 5120 (256 kHz/50 Hz) and for 60 Hz networks is approximately 4267 (256 kHz/60 Hz). The length of the registers enables the measurement of line frequencies as low as 3.9 Hz (256 kHz/2^{16}). The period registers are stable at ±1 LSB when the line is established and the measurement does not change.

The following equations can be used to compute the line period and frequency using the period registers:

$$T_L = \frac{PERIOD[15:0]}{256E3}[\text{sec}] \quad (15)$$

$$f_L = \frac{256E3}{PERIOD[15:0]}[\text{Hz}] \quad (16)$$

Phase Voltage Sag Detection

The ADE7978 can be programmed to detect when the absolute value of any phase voltage drops below or grows above a certain peak value for a number of half-line cycles. The phase where this event takes place and the state of the phase voltage relative to the threshold is identified in Bits[14:12] (VSPHASE[x]) of the PHSTATUS register. An associated interrupt is triggered when any phase drops below or grows above a threshold. This condition is illustrated in Figure 46.

Figure 46 shows Phase A voltage falling below a threshold that is set in the SAG level register (SAGLVL) for four half-line cycles (SAGCYC = 4). When Bit 16 (SAG) in the STATUS1 register is set to 1 to indicate the condition, Bit VSPHASE[0] in the PHSTATUS register is also set to 1 because the phase A voltage is below SAGLVL. The microcontroller then writes back STATUS1 register with Bit 16 (SAG) set to 1 to erase the bit and bring $\overline{\text{IRQ1}}$ interrupt pin back high. Then the phase A voltage stays above the SAGLVL threshold for four half-line cycles (SAGCYC = 4). The Bit 16 (SAG) in STATUS1 register is set to 1 to indicate the condition and the bit VSPHASE[0] in the PHSTATUS register is set back to 0.

Bits VSPHASE[1] and VSPHASE[2] relate to the sag events on Phase B and Phase C in the same way: when Phase B or Phase C voltage stays below SAGLVL, they are set to 1. When the phase voltages are above SAGLVL, they are set to 0.

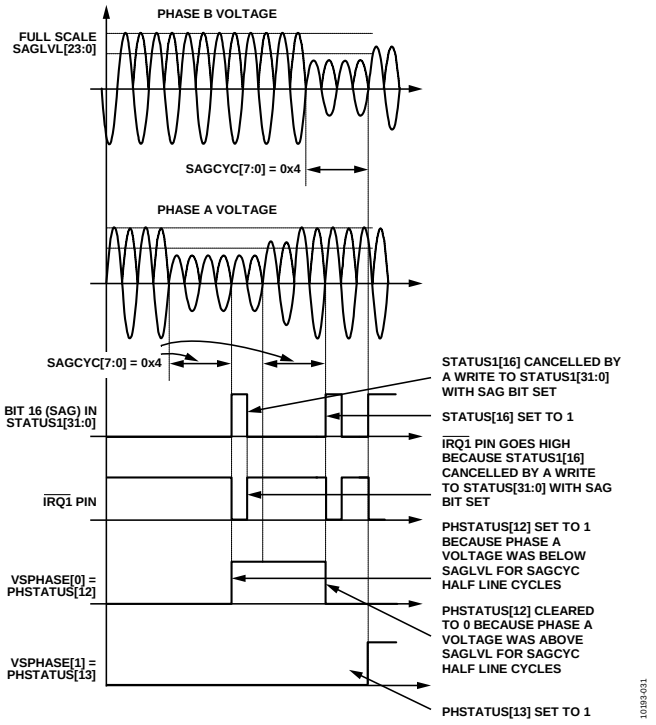


Figure 46. SAG Detection

The SAGCYC register represents the number of half-line cycles the phase voltage must remain below or above the level indicated in the SAGLVL register to trigger a SAG interrupt ; 0 is not a valid number for SAGCYC. For example, when the SAG cycle (SAGCYC[7:0]) contains 0x07, the SAG flag in the STATUS1 register is set at the end of the seventh half line cycle for which the line voltage falls below the threshold. If Bit 16 (SAG) in MASK1 is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low in case of a SAG event in the same moment the Status Bit 16 (SAG) in STATUS1 register is set to 1. The SAG status bit in the STATUS1 register and the $\overline{\text{IRQ1}}$ pin is returned to high by writing to the STATUS1 register with the status bit set to 1.

When the Phase B voltage falls below the indicated threshold into the SAGLVL register for two line cycles, Bit VSPHASE[1] in the PHSTATUS register is set to 1 (see Figure 46). Simultaneously, Bit 16 (SAG) in the STATUS1 register is set to 1 to indicate the condition.

Note that the internal zero-crossing counter is always active. By setting the SAGLVL register, the first SAG detection result is, therefore, not executed across a full SAGCYC period. Writing to the SAGCYC register when the SAGLVL register is already initialized resets the zero-crossing counter, thus ensuring that the first SAG detection result is obtained across a full SAGCYC period.

The recommended procedure to manage SAG events is the following:

1. Enable SAG interrupts in the MASK1 register by setting Bit 16 (SAG) to 1.
2. When a SAG event happens, the $\overline{\text{IRQ1}}$ interrupt pin goes low and Bit 16 (SAG) in the STATUS1 is set to 1.
3. The STATUS1 register is read with Bit 16 (SAG) set to 1.
4. The PHSTATUS register is read, identifying on which phase or phases a SAG event happened.
5. The STATUS1 register is written with Bit 16 (SAG) set to 1. Immediately, the SAG bit is erased.

SAG Level Set

The content of the SAGLVL[23:0] SAG level register is compared to the absolute value of the output from HPF. Writing 5,320,000 to the SAGLVL register, puts the SAG detection level at full scale (see the Voltage Channel ADC section), thus; the SAG event is triggered continuously. Writing 0x00 or 0x01 puts the SAG detection level at 0, therefore, the SAG event is never triggered.

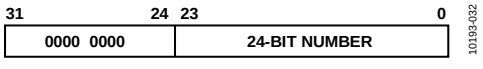


Figure 47. SAGLVL Register Transmitted as a 32-Bit Word

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words. The SAGLVL register is accessed as a 32-bit register with eight MSBs padded with 0s. See Figure 47 for details.

Peak Detection

The ADE7978 records the maximum absolute values reached by the phase voltage and current channels over a certain number of half-line cycles and stores them into the less significant 24 bits of the VPEAK and IPEAK 32-bit registers.

The PEAKCYC register contains the number of half-line cycles used as a time base for the measurement. The circuit uses the zero-crossing points identified by the zero-crossing detection

circuit. Bits[4:2] (PEAKSEL[2:0]) in the MMODE register select the phases upon which the peak measurement is performed. Bit 2 selects Phase A, Bit 3 selects Phase B, and Bit 4 selects Phase C. Selecting more than one phase to monitor the peak values decreases proportionally the measurement period indicated in the PEAKCYC register because zero crossings from more phases are involved in the process. When a new peak value is determined, one of Bits[26:24] (IPPHASE[2:0] or VPPHASE[2:0]) in the IPEAK and VPEAK registers is set to 1, identifying the phase that triggered the peak detection event. For example, if a peak value has been identified on Phase A current, Bit 24 (IPPHASE[0]) in the IPEAK register is set to 1. If next time a new peak value is measured on Phase B, Bit 24 (IPPHASE[0]) of the IPEAK register is cleared to 0, and Bit 25 (IPPHASE[1]) of the IPEAK register is set to 1. Figure 48 shows the composition of the IPEAK and VPEAK registers.

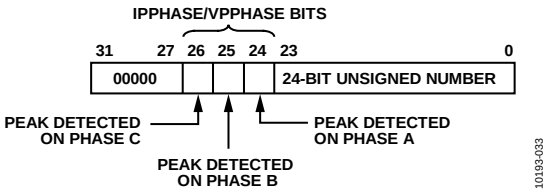


Figure 48. Composition of IPEAK[31:0] and VPEAK[31:0] Registers

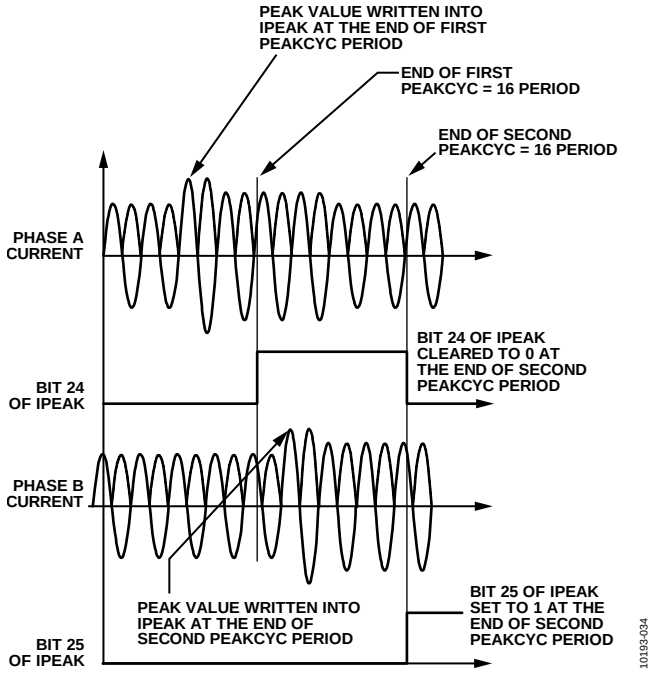


Figure 49. Peak Level Detection

Figure 49 shows how the ADE7978 records the peak value on the current channel when measurements on Phase A and Phase B are enabled (Bit PEAKSEL[2:0] in the MMODE register are 011). PEAKCYC is set to 16, meaning that the peak measurement cycle is four line periods. The maximum absolute value of Phase A is the greatest during the first four line periods (PEAKCYC = 16), so the maximum absolute value is written into the less significant 24 bits of the IPEAK register, and Bit 24 (IPPHASE[0]) of the IPEAK register is set to 1 at the end of the period. This bit remains at 1 for the duration of the second PEAKCYC period of four line cycles. The maximum absolute value of Phase B is the greatest during the second PEAKCYC period; therefore, the maximum absolute value is written into the less significant 24 bits of the IPEAK register, and Bit 25 (IPPHASE[1]) in the IPEAK register is set to 1 at the end of the period.

At the end of the peak detection period in the current channel, Bit 23 (PKI) in the STATUS1 register is set to 1. If Bit 23 (PKI) in the MASK1 register is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low at the end of the PEAKCYC period, and Status Bit 23 (PKI) in the STATUS1 register is set to 1. In a similar way, at the end of the peak detection period in the voltage channel, Bit 24 (PKV) in the STATUS1 register is set to 1. If Bit 24 (PKV) in the MASK1 register is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low at the end of PEAKCYC period and Status Bit 24 (PKV) in the STATUS1 register is set to 1. To find the phase that triggered the interrupt, one of either the IPEAK or VPEAK registers is read immediately after reading the STATUS1 register. Next, the status bits are cleared, and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the status bit set to 1.

Note that the internal zero-crossing counter is always active. By setting Bits[4:2] (PEAKSEL[2:0]) in the MMODE register, the first peak detection result is, therefore, not executed across a full PEAKCYC period. Writing to the PEAKCYC register when the PEAKSEL[2:0] bits are set resets the zero-crossing counter, thereby ensuring that the first peak detection result is obtained across a full PEAKCYC period.

Overvoltage and Overcurrent Detection

The ADE7978 detects when the instantaneous absolute value measured on the phase voltage and current channels becomes greater than the thresholds set in the OVLVL and OILVL 24-bit unsigned registers. If Bit 18 (OV) in the MASK1 register is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low in case of an overvoltage event. There are two status flags set when the $\overline{\text{IRQ1}}$ interrupt pin is driven low: Bit 18 (OV) in the STATUS1 register and one of Bits[11:9] (OVPHASE[2:0]) in the PHSTATUS register to identify the phase that generated the overvoltage. The Status Bit 18 (OV) in the STATUS1 register and all Bits[11:9] (OVPHASE[2:0]) in the PHSTATUS register are cleared, and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the status bit set to 1. Figure 50 presents overvoltage detection in the Phase A voltage.

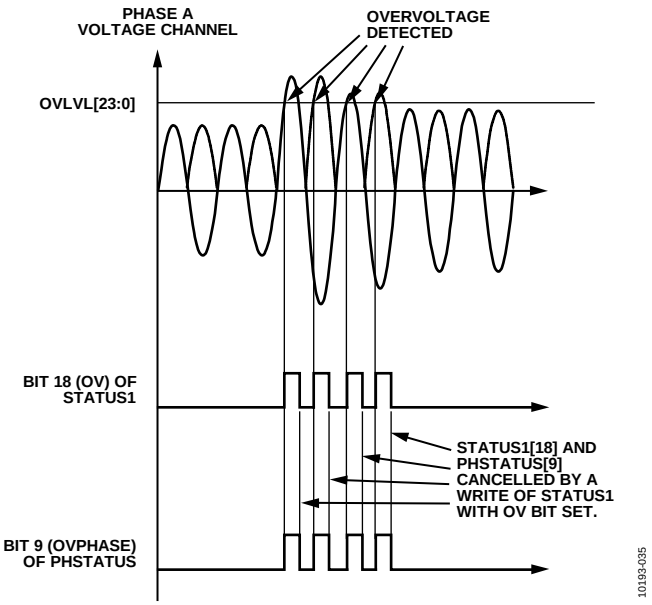


Figure 50. Overvoltage Detection

Whenever the absolute instantaneous value of the voltage goes above the threshold from the OVLVL register, Bit 18 (OV) in the STATUS1 register and Bit 9 (OVPHASE[0]) in the PHSTATUS register are set to 1. Bit 18 (OV) of the STATUS1 register and Bit 9 (OVPHASE[0]) in the PHSTATUS register are cancelled when the STATUS1 register is written with Bit 18 (OV) set to 1.

The recommended procedure to manage overvoltage events is the following:

1. Enable OV interrupts in the MASK1 register by setting Bit 18 (OV) to 1.
2. When an overvoltage event happens, the $\overline{\text{IRQ1}}$ interrupt pin goes low.
3. The STATUS1 register is read with Bit 18 (OV) set to 1.
4. The PHSTATUS register is read, identifying on which phase or phases an overvoltage event happened.
5. The STATUS1 register is written with Bit 18 (OV) set to 1. In this moment, Bit OV is erased and also all Bits[11:9] (OVPHASE[2:0]) of the PHSTATUS register.

In case of an overcurrent event, if Bit 17 (OI) in the MASK1 register is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low. Immediately, Bit 17 (OI) in the STATUS1 register and one of Bits[5:3] (OIPHASE[2:0]) in the PHSTATUS register, which identify the phase that generated the interrupt, are set. To find the phase that triggered the interrupt, the PHSTATUS register is read immediately after reading the STATUS1 register. Next, Status Bit 17 (OI) in the STATUS1 register and Bits[5:3] (OIPHASE[2:0]) in the PHSTATUS register are cleared and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the status bit set to 1. The process is similar with overvoltage detection.

Overvoltage and Overcurrent Level Set

The content of the overvoltage (OVLVL), and overcurrent, (OILVL) 24-bit unsigned registers is compared to the absolute value of the voltage and current channels. The maximum value of these registers is the maximum value of the HPF outputs: 5,320,000. When the OVLVL or OILVL register is equal to this value, the overvoltage or overcurrent conditions are never detected. Writing 0x0 to these registers signifies the overvoltage or overcurrent conditions are continuously detected, and the corresponding interrupts are permanently triggered.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words. Similar to the register presented in Figure 47, OILVL and OVLVL registers are accessed as 32-bit registers with the eight MSBs padded with 0s.

Neutral Current Mismatch

In 3-phase systems, the neutral current is equal to the algebraic sum of the phase currents

$$I_N(t) = I_A(t) + I_B(t) + I_C(t)$$

If there is a mismatch between these two quantities, then a tamper situation may have occurred in the system.

The ADE7978 computes the sum of the phase currents adding the content of the IAWV, IBWV, and ICWV registers, and storing the result into the ISUM 28-bit signed register: $I_{SUM}(t) = I_A(t) + I_B(t) + I_C(t)$. ISUM is computed every 125 µs (8 kHz frequency), the rate at which the current samples are available, and Bit 17 (DREADY) in the STATUS0 register is used to signal when the ISUM register can be read. See the Digital Signal Processor section for more details on Bit DREADY.

To recover $I_{SUM}(t)$ value from the ISUM register, use the following equation:

$$I_{SUM}(t) = \frac{ISUM[27:0]}{ADC_{MAX}} \times I_{FS}$$

where:
ADC_{MAX} =5,320,000, the ADC output when the input is at full scale.
I_{FS} is the full-scale ADC phase current.

Note that the ADE7978 also computes the rms of ISUM and stores it into NIRMS register when Bit 14 (INSEL) in CONFIG register is set to 1 (see Current RMS Calculation section for details).

When bits 5,4 (CONSEL) in the ACCMODE register are set to 01 (meter functions in a 3 wire delta configuration), the Phase B ADE7913 is not connected and the IBWV coming out from the HPF is 0. In this case, ISUM represents a negative estimation of the phase B current (-IBWV) and NIRMS register contains the rms value of the phase B current when Bit 14 (INSEL) in CONFIG register is set to 1.

The ADE7978 computes the difference between the absolute values of ISUM and the neutral current from the INWV

register, takes its absolute value and compares it against the ISUMLVL threshold.

If

$$\left||ISUM|-|INWV|\right| \le ISUMLVL,$$

then it is assumed that the neutral current is equal to the sum of the phase currents, and the system functions correctly.

If

$$\left||ISUM|-|INWV|\right| > ISUMLVL,$$

then a tamper situation may have occurred, and Bit 20 (MISMTCH) in the STATUS1 register is set to 1. An interrupt attached to the flag can be enabled by setting Bit 20 (MISMTCH) in the MASK1 register. If enabled, the $\overline{\text{IRQ1}}$ pin is set low when Status Bit MISMTCH is set to 1. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set back to high by writing to the STATUS1 register with Bit 20 (MISMTCH) set to 1.

If $\left||ISUM|-|INWV|\right| \le ISUMLVL$, then $MISMTCH = 0$

If $\left||ISUM|-|INWV|\right| > ISUMLVL$, then $MISMTCH = 1$

ISUMLVL, the positive threshold used in the process, is a 24-bit signed register. Because it is used in a comparison with an absolute value, always set ISUMLVL as a positive number, somewhere between 0x00000 and 0x7FFFFF. ISUMLVL uses the same scale of the current ADCs outputs, so writing 5,320,000 to the ISUMLVL register puts the mismatch detection level at full scale; see the Current Channel ADC section for details. Writing 0x000000, the default value, or a negative value, signifies the MISMTCH event is always triggered. The right value for the application should be written into the ISUMLVL register after power-up or after a hardware/software reset to avoid continuously triggering MISMTCH events.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. As presented in Figure 51, ISUM, the 28-bit signed register, is accessed as a 32-bit register with the four most significant bits padded with 0s.

Figure 51. The ISUM[27:0] Register is Transmitted As a 32-Bit Word

Similar to the registers presented in Figure 33, the ISUMLVL register is accessed as a 32-bit register with four most significant bits padded with 0s and sign extended to 28 bits.

PHASE COMPENSATION

As described in the Current Channel ADC and Voltage Channel ADC sections, the data path for both phase current and voltages is the same. There is no phase error between phase current and voltage signals introduced by the ADE7978. In addition, shunts are used to sense the phase currents with the ADE7933/ADE7932s, making the phase compensation typically not required.

The ADE7978 provides a means of digitally calibrating eventual phase mismatch errors. The ADE7978 allows a small time delay or time advance to be introduced into the signal processing chain to compensate for the small phase errors.

The phase calibration registers (APHCAL, BPHCAL, and CPHCAL) are 10-bit registers that can vary the time advance in the voltage channel signal path from −374.0 µs to +374.0 µs. Negative values written to the PHCAL registers represent a time advance whereas positive values represent a time delay. One LSB is equivalent to 0.976 µs of time delay or time advance (clock rate of 1.024 MHz). With a line frequency of 60 Hz, this gives a phase resolution of 0.0211° (360° × 60 Hz/1.024 MHz) at the fundamental. This corresponds to a total correction range of −8.079° to +8.079° at 60 Hz. At 50 Hz, the correction range is −6.732° to +6.732° and the resolution is 0.0176° (360° × 50 Hz/1.024 MHz).

Given a phase error of x degrees, measured using the phase voltage as the reference, the corresponding LSBs are computed dividing x by the phase resolution (0.0211°/LSB for 60 Hz and 0.0176°/LSB for 50 Hz). Results between −383 and +383 only are acceptable; numbers outside this range are not accepted. If the current leads the voltage, the result is negative and the absolute value is written into the PHCAL registers. If the current lags the voltage, the result is positive and 512 is added to the result before writing it into xPHCAL.

APHCAL, *BPHCAL*, or *CPHCAL* =

$$\begin{cases} \left|\dfrac{x}{phase\_resolution}\right|, x \le 0 \\ \dfrac{x}{phase\_resolution} + 512, x > 0 \end{cases} \quad (17)$$

Figure 53 illustrates how the phase compensation is used to remove x = −1° phase lead in IA of the current channel from the external current transducer (equivalent of 55.5 µs for 50 Hz systems). To cancel the lead (1°) in the current channel of Phase A, a phase lead must be introduced into the corresponding voltage channel. Using Equation (17), APHCAL is 57 least significant bits, rounded up from 56.8. The phase lead is achieved by introducing a time delay of 55.73 µs into the Phase A current.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words. As shown in Figure 52, APHCAL, BPHCAL, and CPHCAL 10-bit registers are accessed as 16-bit registers with the six MSBs padded with 0s.

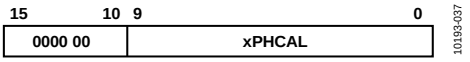


Figure 52. xPHCAL Registers Communicated As 16-Bit Registers

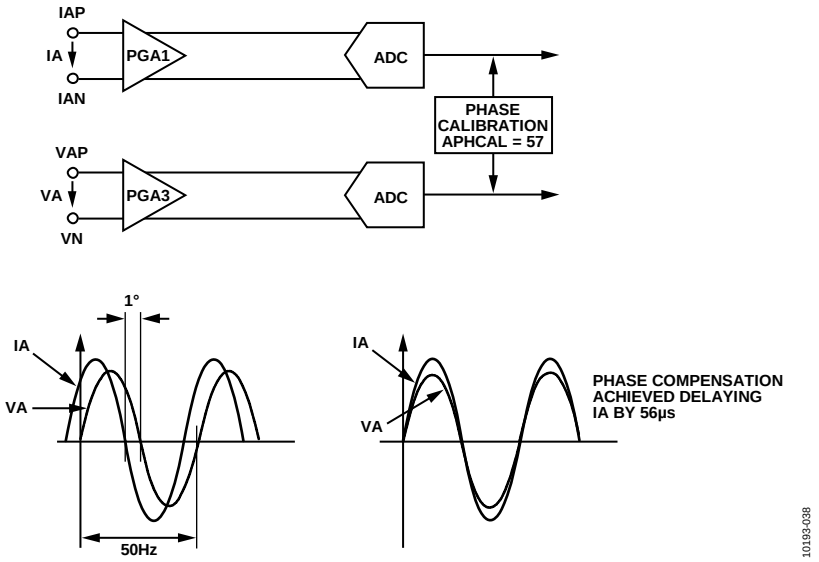


Figure 53. Phase Calibration on Voltage Channels

REFERENCE CIRCUITS

The nominal reference voltage at the REF pin of the ADE7933/ADE7932 is 1.2 ± 0.075% V. The voltage of the ADE7933/ADE7932 reference drifts slightly with temperature; see the ADE7933/ADE7932 Specifications section for the temperature coefficient specification (in ppm/°C). The value of the temperature drift varies from part to part. Because the reference is used for both phase current and voltage ADCs, any x% drift in the reference results in a 2x% deviation of the meter accuracy. The reference drift resulting from temperature changes is usually very small and typically much smaller than the drift of other components on a meter. Alternatively, the meter can be calibrated at multiple temperatures.

The VA2, VB2, VC2, and VN2 voltages and the temperature sensor use the third ADC of the ADE7933/ADE7932, so any x% drift in the reference results in a x% deviation of these measurements.

DIGITAL SIGNAL PROCESSOR

The ADE7978 contains a fixed function digital signal processor (DSP) that computes all powers and rms values. It contains program memory ROM and data memory RAM.

The program used for the power and rms computations is stored in the program memory ROM and the processor executes it every 8 kHz. The end of the computations is signaled by setting Bit 17 (DREADY) to 1 in the STATUS0 register. An interrupt attached to this flag can be enabled by setting Bit 17 (DREADY) in the MASK0 register. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and Status Bit DREADY is set to 1 at the end of the computations. The status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to high by writing to the STATUS0 register with Bit 17 (DREADY) set to 1. Additionally, ZX/$\overline{\text{DREADY}}$ pin, when $\overline{\text{DREADY}}$ functionality is selected, goes low 6.5µs before bit DREADY being set to 1. It stays low for 10µs and then goes back high. Use its low to high transition to initiate a burst read of the waveform sample registers. See I²C Burst Read Operation and SPI Burst Read Operation sections for details. $\overline{\text{DREADY}}$ pin functionality is selected by setting bits 1,0 (ZX_DREADY) to 00 in CONFIG register.

The registers used by the DSP are located in the data memory RAM, at addresses between 0x4380 and 0x43BF. The width of this memory is 28 bits. Within the DSP core, the DSP contains a two stage pipeline. This means that when a single register needs to be initialized, two more writes are required to ensure the value has been written into RAM, and if two or more registers need to be initialized, the last register must be written two more times to ensure the value has been written into RAM.

As explained in the Power Up P section, at power-up or after a hardware or software reset, the DSP is in idle mode. No instruction is executed. All the registers located in the data memory RAM are initialized at 0, their default values, and they can be read/written without any restriction. The run register, used to start and stop the DSP, is cleared to 0x0000. The run register needs to be written with 0x0001 for the DSP to start code execution. It is recommended to first initialize all ADE7978 registers located in the data memory RAM with their desired values. Next, write the last register in the queue two additional times to flush the pipeline, and then write the run register with 0x0001. In this way, the DSP starts the computations from a desired configuration.

To protect the integrity of the data stored in the data memory RAM of the DSP (addresses between 0x4380 and 0x43BF), a write protection mechanism is available. By default, the protection is disabled and registers placed between 0x4380 and

0x43BF can be written without restriction. When the protection is enabled, no writes to these registers is allowed. Registers can be always read, without restriction, independent of the write protection state.

To enable the protection, write 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.

It is recommended to enable the write protectionafter the registers have been initialized. If any data memory RAM based register needs to be changed, simply disable the protection, change the value and then re-enable the protection. There is no need to stop the DSP to change these registers.

To disable the protection, write 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x00 to an internal 8-bit register located at Address 0xE7E3.

The recommended procedure to initialize the registers located in the data memory RAM is as follows:

- Initialize all the ADE7978 registers. First initialize the DSP RAM based registers located between addresses 0x4380 and 0x43BF. Then write the last register in the queue three times. Then initialize the hardware-based configuration registers located between addresses 0xE507 and 0xEA04.
- Enable the write protection by writing 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.
- Read back all data memory RAM registers to ensure they were initialized with the desired values.
- In the remote case that one or more registers are not initialized correctly, disable the protection by writing 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x00 to an internal 8-bit register located at Address 0xE7E3. Reinitialize the registers. Write the last register in the queue three times. Enable the write protection by writing 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.
- Start the DSP by setting run = 1.

There is no obvious reason to stop the DSP. All ADE7978 registers, including ones located in the data memory RAM, can be modified without stopping the DSP. However, to stop the DSP, 0x0000 has to be written into run register. To restart the DSP, one of the following procedures must be followed:

- If the ADE7978 registers located in the data memory RAM have not been modified, write 0x0001 into the run register to start the DSP.
- If the ADE7978 registers located in the data memory RAM have to be modified, first execute a software or a hardware reset, initialize all ADE7978 registers at desired values, enable the write protection, and then write 0x0001 into the run register to start the DSP.

ROOT MEAN SQUARE MEASUREMENT

Root mean square (rms) is a measurement of the magnitude of an ac signal. Its definition can be both practical and mathematical. Defined practically, the rms value assigned to an ac signal is the amount of dc required to produce an equivalent amount of power in the load. Mathematically, the rms value of a continuous signal f(t) is defined as

$$F\,rms = \sqrt{\frac{1}{t}\int_0^t f^2(t)dt} \tag{18}$$

For time sampling signals, rms calculation involves squaring the signal, taking the average, and obtaining the square root.

$$F\,rms = \sqrt{\frac{1}{N}\sum_{N=1}^{N} f^2[n]} \tag{19}$$

Equation (19) implies that for signals containing harmonics, the rms calculation contains the contribution of all harmonics, not only the fundamental.

The method the ADE7978 uses to compute the rms values is to low-pass filter the square of the input signal (LPF) and take the square root of the result (see Figure 54).

$$f(t) = \sum_{k=1}^{\infty} F_k \sqrt{2}\sin\left(k\omega t + \gamma_k\right) \tag{20}$$

Then

$$f^2(t) = \sum_{k=1}^{\infty} F_k^2 - \sum_{k=1}^{\infty} F_k^2 \cos(2k\omega t + 2\gamma_k) + \\ + 2\sum_{\substack{k,m=1 \\ k\neq m}}^{\infty} 2\times F_k \times F_m \sin\left(k\omega t + \gamma_k\right)\times\sin\left(m\omega t + \gamma_m\right) \tag{21}$$

After the LPF and the execution of the square root, the rms value of f(t) is obtained by

$$F = \sqrt{\sum_{k=1}^{\infty} F_k^2} \tag{22}$$

The rms calculation based on this method is simultaneously processed on all current and voltage input channels. Each result is available in the 24-bit registers: AIRMS, BIRMS, CIRMS, NIRMS, AVRMS, BVRMS, CVRMS, NVRMS, AV2RMS, BV2RMS, CV2RMS, and NV2RMS.

In addition, the ADE7978 computes the fundamental rms value of the phase currents and voltages and makes them available in the 24-bit registers: AFIRMS, BFIRMS, CFIRMS, AFVRMS, BFVRMS and CFVRMS.

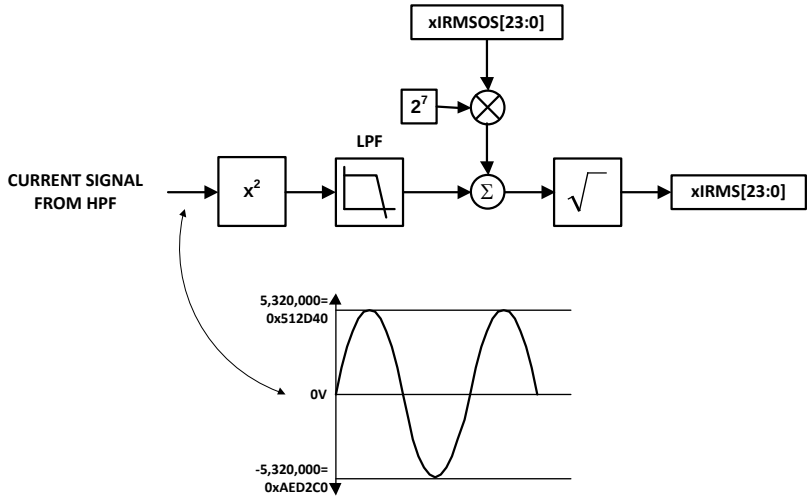


Figure 54. Current RMS Signal Processing

Current RMS Calculation

This section presents how the rms values of all phase and neutral currents are computed.

Figure 54 shows the detail of the signal processing chain for the rms calculation on one of the phases of the current channel. The current channel rms value is processed from the samples used in the current channel. The current rms values are signed 24-bit values and they are stored into the AIRMS, BIRMS, CIRMS, and NIRMS registers.The rms values of the fundamental components are stored into the AFIRMS, BFIRMS, and CFIRMS registers. The update rate of the current rms measurement is 8 kHz. If Bit 14 (INSEL) of the CONFIG register is 0 (default), the NIRMS register contains the rms value of the neutral current. If the INSEL bit is 1, the NIRMS register contains the rms value of the sum of the instantaneous values of the phase currents. Note that in 3-phase three wire delta configuration, the phase B current is not measured and its estimated rms value is equal to NIRMS when INSEL bit is 1. See Neutral Current Mismatch for more details.

With the specified full-scale analog input signal of 0.5 V, the ADC produces an output code that is approximately 5,320,000. The equivalent rms value of a full-scale sinusoidal signal is 3,761,808, independent of the line frequency.

The accuracy of the current rms is typically 0.1% error from the full-scale input down to 1/1000 of the full-scale input. Additionally, this measurement has a bandwidth of 3.3 kHz. It is recommended to read the rms registers synchronous to the voltage zero crossings to ensure stability. The $\overline{\text{IRQ1}}$ interrupt or the ZX functionality at ZX/$\overline{\text{DREADY}}$ can be used to indicate when a zero crossing has occurred (see the **Interrupts** section). The settling time for the I rms measurement is 580msec for both 50Hz and 60Hz input signals. The I rms measurement settling time is the time it takes for the rms register to reflect the value at the input to the current channel when starting from 0.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words. The AIRMS, BIRMS, CIRMS, NIRMS, AFIRMS, BFIRMS, and CFIRMS 24-bit signed registers are accessed as 32-bit registers with the eight MSBs padded with 0s (Figure 55).

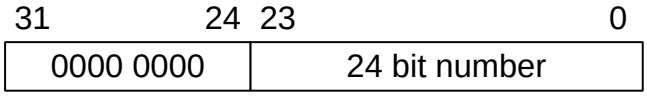


Figure 55. 24-Bit AIRMS, BIRMS, CIRMS and NIRMS Registers transmitted as 32-Bit Words

Current RMS Offset Compensation

The ADE7978 incorporates a current rms offset compensation register for each phase: AIRMSOS, AFIRMSOS, BIRMSOS, BFIRMSOS, CIRMSOS, CFIRMSOS, and NIRMSOS registers. These are 24-bit signed registers that are used to remove offsets in the current rms calculations. An offset can exist in the rms calculation due to input noises that are integrated in the dc component of $I^2(t)$. The current rms offset compensation register is shifted left by 7 bits and then it is added to the squared current rms before the square root is executed. Assuming that the maximum value from the current rms calculation is 3,761,808 with full-scale ac inputs (50 Hz or 60 Hz), one LSB of the current rms offset represents 0.00045% $((\sqrt{3761^2+128}/3761-1)\times 100)$ of the rms measurement at 60 dB down from full scale. Conduct offset calibration at low current; avoid using currents equal to zero for this purpose.

$$I\,rms=\sqrt{I\,rms_0^2+128\times IRMSOS} \quad (23)$$

where $I\,rms_0$ is the rms measurement without offset correction.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to the register presented in Figure 33, the AIRMSOS, AFIRMSOS, BIRMSOS, BFIRMSOS, CIRMSOS, CFIRMSOS, and NIRMSOS 24-bit signed registers are accessed as 32-bit registers with four MSBs padded with 0s and sign extended to 28 bits.

Voltage Channel RMS Calculation

Figure 56 shows the detail of the signal processing chain for the rms calculation on one of the phases of the voltage channels. The voltage channel rms value is processed from the samples used in the voltage channel. The voltage rms values are signed 24-bit values and they are stored into the Registers AVRMS, AV2RMS, BVRMS, BV2RMS, CVRMS, CV2RMS, NVRMS and NV2RMS. The rms values of the fundamental components are stored into the AFVRMS, BFVRMS, and CFVRMS registers. The update rate of the current rms measurement is 8 kHz.

With the specified full-scale analog input signal of 0.5 V, the ADC produces an output code that is approximately 5,320,000. The equivalent rms value of a full-scale sinusoidal signal is 3,761,808, independent of the line frequency.

The accuracy of the voltage rms is typically 0.1% error from the full-scale input down to 1/1000 of the full-scale input. Additionally, this measurement has a bandwidth of 3.3 kHz. It is recommended to read the rms registers synchronous to the voltage zero crossings to ensure stability. The $\overline{\text{IRQ1}}$ interrupt can be used to indicate when a zero crossing has occurred (see the Interrupts section).

The settling time for the V rms measurement is 580 ms for both 50 Hz and 60 Hz input signals. The V rms measurement settling time is the time it takes for the rms register to reflect the value at the input to the voltage channel when starting from 0.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words. Similar to the register presented in Figure 47, the AVRMS, AFVRMS, AV2RMS, BVRMS, BFVRMS, BV2RMS, CVRMS, CFVRMS, CV2RMS, NVRMS and NV2RMS 24-bit signed registers are accessed as 32-bit registers with the eight MSBs padded with 0s.

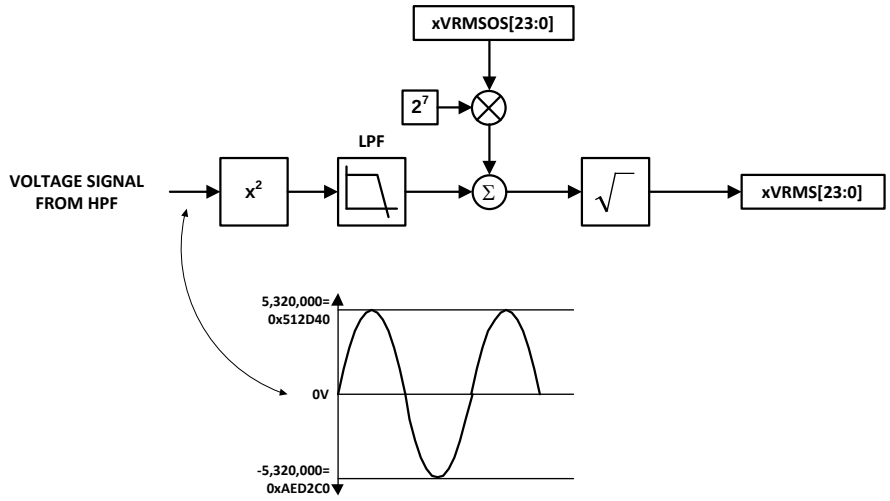


Figure 56. Voltage RMS Signal Processing

Voltage RMS Offset Compensation

The ADE7978 incorporates voltage rms offset compensation registers for each voltage: AVRMSOS, AFVRMSOS, AV2RMSOS, BVRMSOS, BFVRMSOS, BV2RMSOS, CVRMSOS, CFVRMSOS, CV2RMSOS, NVRMSOS, and NV2RMSOS. These are 24-bit signed registers used to remove offsets in the voltage rms calculations. An offset can exist in the rms calculation due to input noises that are integrated in the dc component of

$V^2(t)$. The voltage rms offset compensation register is shifted left by 7 bits and then it is added to the squared voltage rms before the square root is executed. Assuming that the maximum value from the voltage rms calculation is 3,761,808 with full-scale ac inputs (50 Hz or 60 Hz), one LSB of the current rms offset represents 0.00045% ($(\sqrt{3761^2+128}/3761-1)\times 100$) of the rms measurement at 60 dB down from full scale. Conduct offset calibration at low current; avoid using voltages equal to zero for this purpose.

$$V\ rms = \sqrt{V\ rms_0^2 + 128 \times VRMSOS} \quad (24)$$

where $V\ rms_0$ is the rms measurement without offset correction.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to registers presented in Figure 33, the AVRMSOS, AFVRMSOS, AV2RMSOS, BVRMSOS, BFVRMSOS, BV2RMSOS, CVRMSOS, CFVRMSOS, CV2RMSOS, NVRMSOS, and NV2RMSOS 24-bit registers are accessed as 32-bit registers with the four most significant bits padded with 0s and sign extended to 28 bits.

Voltage RMS in 3-Phase Three Wire Delta Configurations

In 3-phase three wire delta configurations, Phase B is considered the ground of the system, and Phase A and Phase C voltages are measured relative to it (see Figure 18). This configuration is chosen using bits 5,4 (CONSEL) equal to 01 in ACCMODE register (see Table 21 for all configurations where the ADE7978 may be used). In this situation, all Phase B active, reactive, and apparent powers are 0.

In this configuration, the ADE7978 computes the rms value of the line voltage between Phase A and Phase C and stores the result into BVRMS register. BFVRMS register contains the rms of the fundamental component of the BVRMS line voltage. BVGAIN, BVRMSOS, and BFVRMSOS registers may be used to calibrate BVRMS and BFVRMS registers computed in this configuration.

ACTIVE POWER CALCULATION

The ADE7978 computes the total active power on every phase. Total active power considers in its calculation all fundamental and harmonic components of the voltages and currents. In addition, the ADE7978 computes the fundamental active power, the power determined only by the fundamental components of the voltages and currents.

Total Active Power Calculation

Electrical power is defined as the rate of energy flow from source to load, and it is given by the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal, and it is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. If an ac system is supplied by a voltage, v(t), and consumes the current, i(t), and each of them contains harmonics, then

$$v(t) = \sum_{k=1}^{\infty} V_k \sqrt{2} \sin(k\omega t + \varphi_k)$$
$$i(t) = \sum_{k=1}^{\infty} I_k \sqrt{2} \sin(k\omega t + \gamma_k) \quad (25)$$

where:
V_k, I_k are rms voltage and current, respectively, of each harmonic.
φ_k, γ_k are the phase delays of each harmonic.

The total active power is equal to the dc component of the instantaneous power signal, that is,

$$\sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k - \gamma_k)$$

This is the equation used to calculate the total active power in the ADE7978 for each phase. The equation of fundamental active power is:

$$FP = V_1 I_1 \cos(\varphi_1 - \gamma_1) \quad (26)$$

Figure 57 shows how the ADE7978 computes the total active power on each phase. First, it multiplies the current and voltage signals in each phase. Next, it extracts the dc component of the instantaneous power signal in each phase (A, B, and C) using LPF2, the low-pass filter.

If the phase currents and voltages contain only the fundamental component, are in phase (that is $\varphi_1 = \gamma_1 = 0$), and they correspond to full-scale ADC inputs, then multiplying them results in an instantaneous power signal that has a dc component, $V_1 \times I_1$, and a sinusoidal component, $V_1 \times I_1 \cos(2\omega t)$; Figure 58 shows the corresponding waveforms.

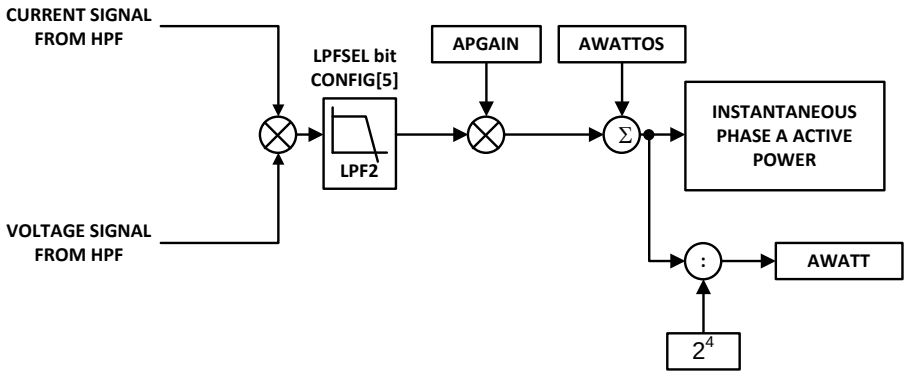


Figure 57. Total Active Power Data Path

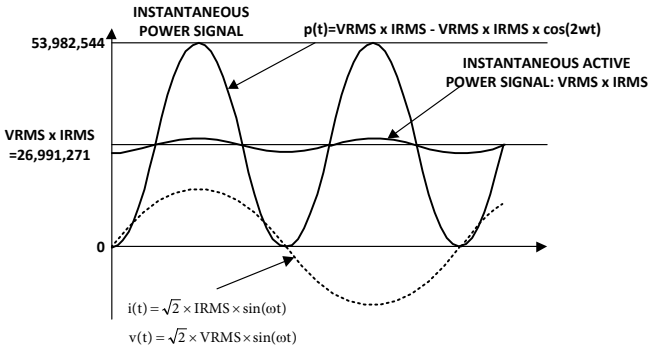


Figure 58. Active Power Calculation

Because LPF2 does not have an ideal brick wall frequency response, the active power signal has some ripple due to the instantaneous power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Because the ripple is sinusoidal in nature, it is removed when the active power signal is integrated over time to calculate the energy. Bit 5 (LPFSEL) of CONFIG register selects the LPF2 strength. If LPFSEL is 0 (default), the settling time is 650 ms and the ripple attenuation is 65 dB. If LPFSEL is 1, the settling time is 1300 ms and the ripple attenuation is 128 dB. Figure 59 shows the frequency response of LPF2 when LPFSEL is 0 and Figure 60 shows the frequency response of LPF2 when LPFSEL is 1.

The ADE7978 stores the instantaneous total phase active powers into the AWATT, BWATT, and CWATT registers. Their equation is

$$xWATT = \sum_{k=1}^{\infty} \frac{V_k}{V_{FS}} \times \frac{I_k}{I_{FS}} \times \cos(\varphi_k - \gamma_k) \times PMAX \times \frac{1}{2^4} \quad (27)$$

where:
V_{FS}, I_{FS} are the rms values of the phase voltage and current when the ADC inputs are at full scale.
$PMAX$ = 26,991,271 it is the instantaneous power computed when the ADC inputs are at full scale and in phase.

The xWATT[23:0] waveform registers can be accessed using various serial ports. Refer to the Waveform Sampling Mode section for more details.

Fundamental Active Power Calculation

The ADE7978 computes the fundamental active power using a proprietary algorithm that requires some initializations function of the frequency of the network and its nominal voltage measured in the voltage channel. Bit 14 (SELFREQ) in the COMPMODE register must be set according to the frequency of the network in which the ADE7978 is connected. If the network frequency is 50 Hz, clear this bit to 0 (the default value). If the network frequency is 60 Hz, set this bit to 1. In addition, initialize the VLEVEL 24-bit signed register with a positive value based on the following equation:

$$VLEVEL = \frac{V_{FS}}{V_n} \times 4 \times 10^6 \quad (28)$$

where:
V_{FS} is the rms value of the phase voltages when the ADC inputs are at full scale.
V_n is the rms nominal value of the phase voltage.

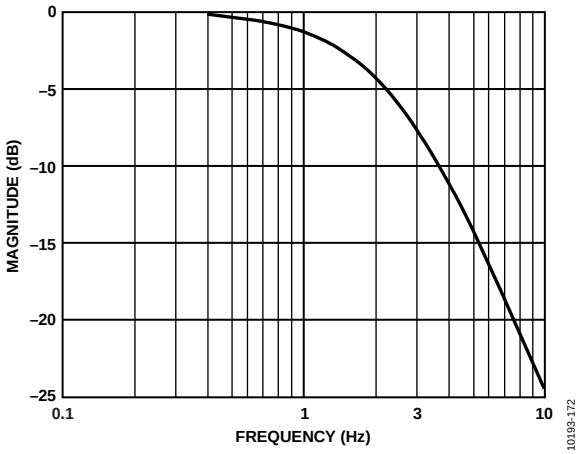


Figure 59. Frequency Response of the LPF Used to Filter Instantaneous Power in Each Phase When the LPFSEL Bit of CONFIG is 0 (Default)

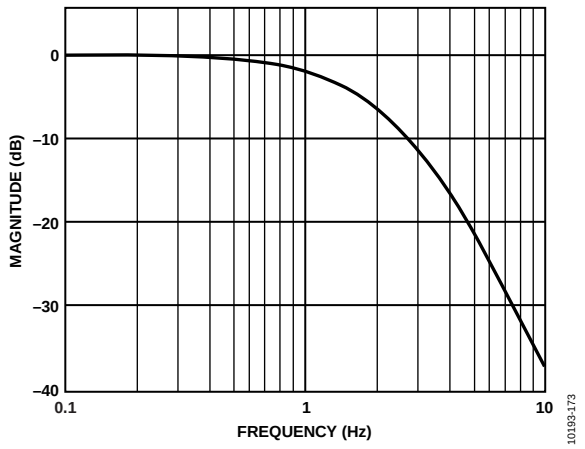


Figure 60. Frequency Response of the LPF Used to Filter Instantaneous Power in Each Phase when the LPFSEL Bit of CONFIG is 1

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to the registers presented in Figure 33, the VLEVEL 24-bit signed register is accessed as a 32-bit register with four most significant bits padded with 0s and sign extended to 28 bits.

Table 19 presents the settling time for the fundamental active power measurement.

Table 19. Settling Time for Fundamental Active Power

Input Signals	
63% PMAX	**100% PMAX**
375 ms	875 ms

Active Power Gain Calibration

Note that the average active power result from the LPF2 output in each phase can be scaled by ±100% by writing to the phase's watt gain 24-bit register (APGAIN, BPGAIN, CPGAIN). The xPGAIN registers are placed on data paths of all powers computed by the ADE7978: total active and reactive powers, fundamental active and reactive powers and apparent powers. This is possible because all power data paths have identical overall gains. Therefore, to compensate the gain errors in various powers data paths it is sufficient to analyze only one power data path, for example the total active power, calculate the correspondent APGAIN, BPGAIN and CPGAIN registers and all the power data paths are gain compensated.

The power gain registers are twos complement, signed registers and have a resolution of 2^{-23}/LSB. Equation (29) describes mathematically the function of the power gain registers.

$$Average\ Power\ Data = LPF2\ Output \times \left(1 + \frac{Power\ Gain\ Register}{2^{23}}\right) \quad (29)$$

The output is scaled by −50% by writing 0xC00000 to the watt gain registers, and it is increased by +50% by writing 0x400000 to them. These registers are used to calibrate the active, reactive and apparent power (or energy) calculation for each phase.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words, and the DSP works on 28 bits. Similar to registers presented in Figure 33, the APGAIN, BPGAIN, and CPGAIN 24-bit signed registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

Active Power Offset Calibration

The ADE7978 incorporates a watt offset 24-bit register on each phase and on each active power. The AWATTOS, BWATTOS, and CWATTOS registers compensate the offsets in the total active power calculations, and the AFWATTOS, BFWATTOS, and CFWATTOS registers compensate offsets in the fundamental active power calculations. These are signed twos complement, 24-bit registers that are used to remove offsets in the active power calculations. An offset can exist in the power calculation due to crosstalk between channels on the PCB or in the chip itself. One LSB in the active power offset register is equivalent to 1 LSB in the active power multiplier output. With full-scale current and voltage inputs, the LPF2 output is PMAX = 26,991,271. At −80 dB down from the full scale (active power scaled down 10^4 times), one LSB of the active power offset register represents 0.037% of PMAX.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to registers presented in Figure 33, the AWATTOS, BWATTOS, CWATTOS, AFWATTOS, BFWATTOS, and CFWATTOS 24-bit signed registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

Sign of Active Power Calculation

The average active power is a signed calculation. If the phase difference between the current and voltage waveform is more than 90°, the average power becomes negative. Negative power indicates that energy is being injected back on the grid. The ADE7978 has sign detection circuitry for active power calculations. It can monitor the total active powers or the fundamental active powers. As described in the Active Energy Calculation section, the active energy accumulation is performed in two stages. Every time a sign change is detected in the energy accumulation at the end of the first stage, that is, after the energy accumulated into the internal accumulator reaches the WTHR register threshold, a dedicated interrupt is triggered. The sign of each phase active power can be read in the PHSIGN register.

Bit 6 (REVAPSEL) in the ACCMODE register sets the type of active power being monitored. When REVAPSEL is 0, the default value, the total active power is monitored. When REVAPSEL is 1, the fundamental active power is monitored.

Bits[8:6] (REVAPC, REVAPB, and REVAPA, respectively) in the STATUS0 register are set when a sign change occurs in the

power selected by Bit 6 (REVAPSEL) in the ACCMODE register.

Bits[2:0] (CWSIGN, BWSIGN, and AWSIGN, respectively) in the PHSIGN register are set simultaneously with the REVAPC, REVAPB, and REVAPA bits. They indicate the sign of the power. When they are 0, the corresponding power is positive. When they are 1, the corresponding power is negative.

Bit REVAPx of STATUS0 and Bit xWSIGN in the PHSIGN register refer to the total active power of Phase x, the power type being selected by Bit 6 (REVAPSEL) in the ACCMODE register.

Interrupts attached to Bits[8:6] (REVAPC, REVAPB, and REVAPA, respectively) in the STATUS0 register can be enabled by setting Bits[8:6] in the MASK0 register. If enabled, the $\overline{\text{IRQ0}}$ pin is set low, and the status bit is set to 1 whenever a change of sign occurs. To find the phase that triggered the interrupt, the PHSIGN register is read immediately after reading the STATUS0 register. Next, the status bit is cleared and the $\overline{\text{IRQ0}}$ pin is returned to high by writing to the STATUS0 register with the corresponding bit set to 1.

Active Energy Calculation

Active energy is defined as the integral of active power.

$$Energy = \int p(t)dt \tag{30}$$

The ADE7978 achieves the integration of the active power signal in two stages (see Figure 61). The process is identical for both total and fundamental active powers. The first stage accumulates the instantaneous phase total or fundamental active power at 1.024MHz, although they are computed by the DSP at 8 kHz rate. Every time a threshold is reached, a pulse is generated and the threshold is subtracted from the internal register.

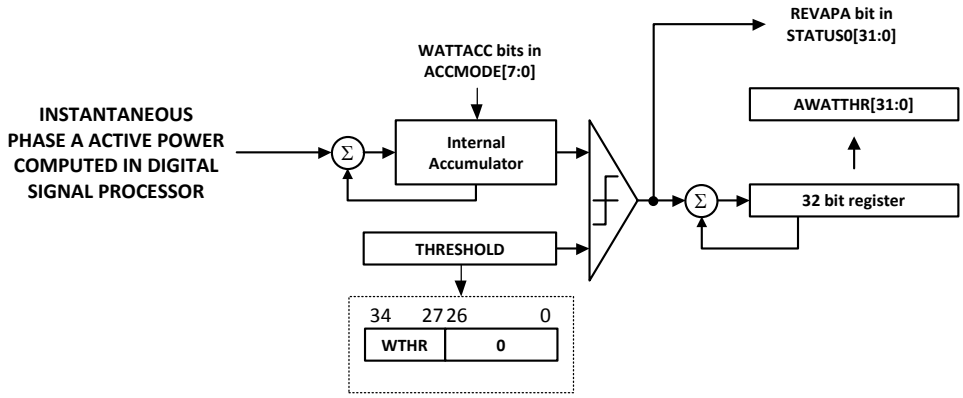


Figure 61. Total Active Energy Accumulation

The sign of the energy in this moment is considered the sign of the active power (see the Sign of Active Power Calculation section for details). The second stage consists of accumulating the pulses generated at the first stage into internal 32-bit accumulation registers. The content of these registers is transferred to watt-hour registers, xWATTHR and xFWATTHR, when these registers are accessed.

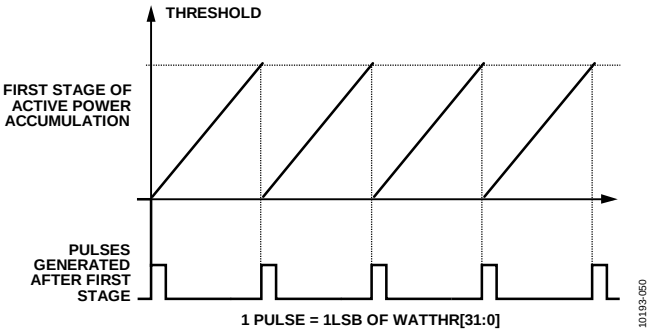


Figure 62. Active Power Accumulation Inside the DSP

Figure 62 explains this process. The threshold is formed by concatenating the WTHR 8-bit unsigned register to 27 bits equal to 0. It is introduced by the user and is common for total active and fundamental powers on all phases. Its value depends on how much energy is assigned to one LSB of watt-hour registers. Supposing a derivative of Wh [10^n Wh], n as an integer, is desired as one LSB of the xWATTHR register, WTHR is computed using the following equation:

$$WTHR = \frac{PMAX \times f_S \times 3600 \times 10^n}{V_{FS} \times I_{FS} \times 2^{27}} \tag{31}$$

where:
$PMAX$ = 26,991,271 = 0x19BDAA7 as the instantaneous power computed when the ADC inputs are at full scale.
f_S = 1.024 MHz, the frequency at which every instantaneous power computed by the DSP at 8 kHz is accumulated.
V_{FS}, I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.

WTHR register is an 8-bit unsigned number, so its maximum value is $2^8 - 1$. Its default value is 0x3. Values lower than 3, that is 2 or 1 should be avoided and 0 should never be used as the threshold must be a non-zero value.

This discrete time accumulation or summation is equivalent to integration in continuous time following the description in Equation (32).

$$Energy = \int p(t)dt = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} p(nT) \times T \right\} \quad (32)$$

where:
n is the discrete time sample number.
T is the sample period.

In the ADE7978, the total phase active powers are accumulated in the AWATTHR, BWATTHR, and CWATTHR 32-bit signed registers, and the fundamental phase active powers are accumulated in AFWATTHR, BFWATTHR, and CFWATTHR 32-bit signed registers. The active energy register content can roll over to full-scale negative (0x80000000) and continue increasing in value when the active power is positive. Conversely, if the active power is negative, the energy register underflows to full-scale positive (0x7FFFFFFF) and continues decreasing in value.

The ADE7978 provides a status flag to signal when one of the xWATTHR and xFWATTHR registers is half full. Bit 0 (AEHF) in the STATUS0 register is set when Bit 30 of one of the xWATTHR registers changes, signifying one of these registers is half full. If the active power is positive, the watt-hour register becomes half full when it increments from 0x3FFF FFFF to 0x4000 0000. If the active power is negative, the watt-hour register becomes half full when it decrements from 0xC000 0000 to 0xBFFF FFFF. Similarly, Bit 1 (FAEHF) in STATUS0 register, is set when Bit 30 of one of the xFWATTHR registers changes, signifying one of these registers is half full.

Setting Bits[1:0] in the MASK0 register enable the FAEHF and AEHF interrupts, respectively. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever one of the energy registers, xWATTHR (for the AEHF interrupt) or xFWATTHR (for the FAEHF interrupt), become half full. The status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to logic high by writing to the STATUS0 register with the corresponding bit set to 1.

Setting Bit 6 (RSTREAD) of the LCYCMODE register enables a read-with-reset for all watt-hour accumulation registers, that is, the registers are reset to 0 after a read operation.

Integration Time Under Steady Load

The discrete time sample period (T) for the accumulation register is 976.5625 ns (1.024MHz frequency). With full-scale sinusoidal signals on the analog inputs and the watt gain registers set to 0x00000, the average word value from each LPF2 is PMAX = 26,991,271. If the WTHR register threshold is set at 3, its minimum recommended value, the first stage accumulator generates a pulse that is added to watt-hour registers every

$$\frac{3 \times 2^{27}}{PMAX \times 1.024 \times 10^6} = 14.5683 \mu\text{sec}$$

The maximum value that can be stored in the watt-hour accumulation register before it overflows is $2^{31} - 1$ or 0x7FFFFFFF. The integration time is calculated as

$$Time = 0x7FFF,FFFF \times 14.5683\ \mu s = 8\ hr\ 41\ min\ 25sec \quad (33)$$

Energy Accumulation Modes

The active power is accumulated in each watt-hour accumulation 32-bit register (AWATTHR, BWATTHR, CWATTHR, AFWATTHR, BFWATTHR, and CFWATTHR) according to the configuration of Bit 5 and Bit 4 (CONSEL bits) in the ACCMODE register. The various configurations are described in Table 20.

Table 20. Inputs to Watt-Hour Accumulation Registers

CONSEL	AWATTHR	BWATTHR	CWATTHR
00	VA × IA	VB × IB	VC × IC
01	VA × IA	VB × IB VB = VA – VC[1]	VC × IC
10	VA × IA	VB × IB VB = –VA – VC	VC × IC
11	VA × IA	VB × IB VB = –VA	VC × IC

[1] In a 3-phase three wire case (CONSEL[1:0] = 01), the ADE7978 computes the rms value of the line voltage between Phase A and Phase C and stores the result into BVRMS register (see the Voltage RMS in 3-Phase Three Wire Delta Configurations section). The Phase B current determined after the HPF is 0. Consequently, the powers associated with Phase B are 0. To avoid any errors in the frequency output pins (CF1, CF2, or CF3) related to the powers associated with Phase B, disable the contribution of Phase B to the energy-to-frequency converters by setting bits TEMSEL1[1] or TERMSEL2[1] or TERMSEL3[1] to 0 in the COMPMODE register (see the Energy-to-Frequency Conversion section).

Depending on the polyphase meter service, choose the appropriate formula to calculate the active energy. The American ANSI C12.10 standard defines the different configurations of the meter. Table 21 describes which mode to choose in these various configurations.

Table 21. Meter Form Configuration

ANSI Meter Form	Configuration	CONSEL
5S/13S	3-wire delta	01
6S/14S	4-wire wye	10
8S/15S	4-wire delta	11
9S/16S	4-wire wye	00

Bits[1:0] (WATTACC[1:0]) in the ACCMODE register determine how the active power is accumulated in the watt-hour registers and how the CF frequency output can be generated as a function of the total and fundamental active powers. See the Energy-to-Frequency Conversion section for details.

Line Cycle Active Energy Accumulation Mode

In line cycle energy accumulation mode, the energy accumulation is synchronized to the voltage channel zero crossings such that active energy is accumulated over an integral number of half line cycles. The advantage of summing the active energy over an integer number of line cycles is that the sinusoidal component in the active energy is reduced to 0. This eliminates any ripple in the energy calculation and allows the energy to be accumulated accurately over a shorter time. By using the line cycle energy accumulation mode, the energy calibration can be greatly simplified, and the time required to calibrate the meter can be significantly reduced. In line cycle energy accumulation

mode, the ADE7978 transfers the active energy accumulated in the 32-bit internal accumulation registers into the xWATHHR or xFWATTHR registers after an integral number of line cycles, as shown in Figure 63. The number of half line cycles is specified in the LINECYC register.

The line cycle energy accumulation mode is activated by setting Bit 0 (LWATT) in the LCYCMODE register. The energy accumulation over an integer number of half line cycles is written to the watt-hour accumulation registers after LINECYC number of half line cycles is detected. When using the line cycle accumulation mode, the Bit 6 (RSTREAD) of the LCYCMODE register should be set to Logic 0 because a read with reset of watt-hour registers outside the LINECYC period resets the energy accumulation.

Phase A, Phase B, and Phase C zero crossings are, respectively, included when counting the number of half line cycles by setting Bits[5:3] (ZXSEL[x]) in the LCYCMODE register. Any combination of the zero crossings from all three phases can be used for counting the zero crossing. Select only one phase at a time for inclusion in the zero crossings count during calibration.

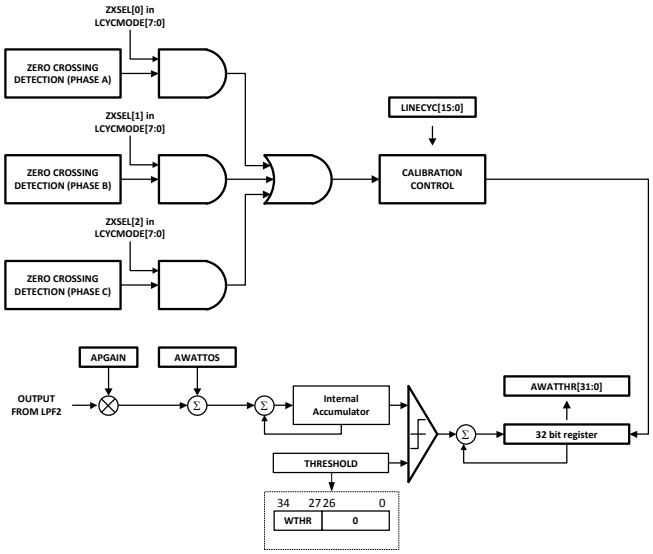


Figure 63. Line Cycle Active Energy Accumulation Mode

The number of zero crossings is specified by the LINECYC 16-bit unsigned register. The ADE7978 can accumulate active power for up to 65,535 combined zero crossings. Note that the internal zero-crossing counter is always active. By setting Bit 0 (LWATT) in the LCYCMODE register, the first energy accumulation result is, therefore, incorrect. Writing to the LINECYC register when the LWATT bit is set resets the zero-crossing counter, thus ensuring that the first energy accumulation result is accurate.

At the end of an energy calibration cycle, Bit 5 (LENERGY) in the STATUS0 register is set. If the corresponding mask bit in the MASK0 interrupt mask register is enabled, the $\overline{\text{IRQ0}}$ pin also goes active low. The status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to high again by writing to the STATUS0 register with the corresponding bit set to 1.

Because the active power is integrated on an integer number of half-line cycles in this mode, the sinusoidal components are reduced to 0, eliminating any ripple in the energy calculation. Therefore, total energy accumulated using the line cycle accumulation mode is

$$e = \int_{t}^{t+nT} p(t)dt = nT\sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k - \gamma_k) \quad (34)$$

where nT is the accumulation time.

Note that line cycle active energy accumulation uses the same signal path as the active energy accumulation. The LSB size of these two methods is equivalent.

REACTIVE POWER CALCULATION

The ADE7978 can compute the total reactive power on every phase. Total reactive power integrates all fundamental and harmonic components of the voltages and currents. The ADE7978 also computes the fundamental reactive power, the power determined only by the fundamental components of the voltages and currents.

A load that contains a reactive element (inductor or capacitor) produces a phase difference between the applied ac voltage and the resulting current. The power associated with reactive elements is called reactive power, and its unit is VAR. Reactive power is defined as the product of the voltage and current waveforms when all harmonic components of one of these signals are phase shifted by 90°.

The total reactive power is equal to:

$$Q = \sum_{k=1}^{\infty} V_k I_k \sin(\varphi_k - \gamma_k) \quad (35)$$

This is the relationship used to calculate the total reactive power in the ADE7978 for each phase. The instantaneous reactive power signal is generated by multiplying each harmonic of the voltage signals by the 90° phase-shifted corresponding harmonic of the current in each phase.

The ADE7978 stores the instantaneous total phase reactive powers into the AVAR, BVAR, and CVAR registers. Their expression is

$$xVAR = \sum_{k=1}^{\infty} \frac{V_k}{V_{FS}} \times \frac{I_k}{I_{FS}} \times \sin(\varphi_k - \gamma_k) \times PMAX \times \frac{1}{2^4} \quad (36)$$

where:
V_{FS}, I_{FS} are the rms values of the phase voltage and current when the ADC inputs are at full scale.
$PMAX$ = 26,991,271, the instantaneous power computed when the ADC inputs are at full scale and in phase.

The xVAR waveform registers can be accessed using various serial ports. Refer to the Waveform Sampling Mode section for more details.

The expression of fundamental reactive power is obtained from Equation (35) with k = 1, as follows:

$$FQ = V_1 I_1 \sin(\varphi_1 - \gamma_1)$$

The ADE7978 computes the fundamental reactive power using a proprietary algorithm that requires some initialization function of the frequency of the network and its nominal voltage measured in the voltage channel. These initializations are introduced in the Active Power Calculation section and are common for both fundamental active and reactive powers.

Table 22 presents the settling time for the fundamental reactive power measurement, which is the time it takes the power to reflect the value at the input of the ADE7978.

Table 22. Settling Time for Fundamental Reactive Power

Input Signals	
63% Full Scale	**100% Full Scale**
375 ms	875 ms

Reactive Power Gain Calibration

The average reactive power in each phase can be scaled by ±100% by writing to one of the phase's VAR gain 24-bit register (APGAIN, BPGAIN, or CPGAIN). Note that these registers are the same gain registers used to compensate the other powers computed by the ADE7978. See Active Power Gain Calibration section for details on these registers.

Reactive Power Offset Calibration

The ADE78978 provides a reactive power offset register on each phase and on each reactive power. AVAROS, BVAROS, and CVAROS registers compensate the offsets in the total reactive power calculations, whereas AFVAROS, BFVAROS, and CFVAROS registers compensate offsets in the fundamental reactive power calculations. These are signed twos complement, 24-bit registers that are used to remove offsets in the reactive power calculations. An offset can exist in the power calculation due to crosstalk between channels on the PCB or in the chip itself. The offset resolution of the registers is the same as for the active power offset registers (see the Active Power Offset Calibration section).

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE78978 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to the registers presented in Figure 33, the AVAROS, BVAROS, and CVAROS 24-bit signed registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

Sign of Reactive Power Calculation

Note that the reactive power is a signed calculation. Table 23 summarizes the relationship between the phase difference between the voltage and the current and the sign of the resulting reactive power calculation.

The ADE7978 has sign detection circuitry for reactive power calculations that can monitor the total reactive powers or the fundamental reactive powers. As described in the Reactive Energy Calculation section, the reactive energy accumulation is executed in two stages. Every time a sign change is detected in the energy accumulation at the end of the first stage, that is, after the energy accumulated into the internal accumulator reaches the VARTHR register threshold, a dedicated interrupt is triggered. The sign of each phase reactive power can be read in the PHSIGN register. Bit 7 (REVRPSEL) in the ACCMODE register sets the type of reactive power being monitored. When REVRPSEL is 0, the default value, the total reactive power is monitored. When REVRPSEL is 1, then the fundamental reactive power is monitored.

Bits[12:10] (REVRPC, REVRPB, and REVRPA, respectively) in the STATUS0 register are set when a sign change occurs in the power selected by Bit 7 (REVRPSEL) in the ACCMODE register.

Bits[6:4] (CVARSIGN, BVARSIGN, and AVARSIGN, respectively) in the PHSIGN register are set simultaneously with the REVRPC, REVRPB, and REVRPA bits. They indicate the sign of the reactive power. When they are 0, the reactive power is positive. When they are 1, the reactive power is negative.

Bit REVRPx of the STATUS0 register and Bit xVARSIGN in the PHSIGN register refer to the reactive power of Phase x, the power type being selected by Bit REVRPSEL in ACCMODE register.

Setting Bits[12:10] in the MASK0 register enables the REVRPC, REVRPB, and REVRPA interrupts, respectively. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever a change of sign occurs. To find the phase that triggered the interrupt, the PHSIGN register is read immediately after reading the STATUS0 register. Next, the status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to high by writing to the STATUS0 register with the corresponding bit set to 1.

Table 23. Sign of Reactive Power Calculation

Φ[1]	Sign of Reactive Power
Between 0 to +180	Positive
Between –180 to 0	Negative

[1] Φ is defined as the phase angle of the voltage signal minus the current signal; that is, Φ is positive if the load is inductive and negative if the load is capacitive.

Reactive Energy Calculation

Reactive energy is defined as the integral of reactive power.

$$Reactive\ Energy = \int q(t)dt \quad (37)$$

Similar to active power, the ADE7978 achieves the integration of the reactive power signal in two stages (see Figure 64).

- The first stage accumulates the instantaneous phase total or fundamental reactive power at 1.024 MHz, although they are computed by the DSP at 8 kHz rate. Every time a threshold is reached, a pulse is generated and the threshold is subtracted from the internal register. The sign of the energy in this moment is considered the sign of the reactive power (see the Sign of Reactive Power Calculation section for details).
- The second stage consists in accumulating the pulses generated by the processor into internal 32-bit

accumulation registers. The content of these registers is transferred to the var-hour registers (xVARHR and xFVARHR) when these registers are accessed. AVARHR, BVARHR, CVARHR, AFVARHR, BFVARHR, and CFVARHR represent phase total and fundamental reactive powers.

Figure 64 explains this process. The threshold is formed by concatenating the VARTHR 8-bit unsigned register to 27 bits equal to 0. It is introduced by the user and is common for total active and fundamental powers on all phases. Its value depends on how much energy is assigned to one LSB of var-hour registers. Supposing a derivative of a volt ampere reactive hour (varh) [10^n varh] where n is an integer, is desired as one LSB of the VARHR register, the VARTHR register can be computed using the following equation:

$$VARTHR = \frac{PMAX \times f_s \times 3600 \times 10^n}{V_{FS} \times I_{FS} \times 2^{27}} \quad (38)$$

where:
$PMAX$ = 26,991,271 = 0x19BDAA7, the instantaneous power computed when the ADC inputs are at full scale.
f_S = 1.024 MHz, the frequency at which every instantaneous power computed by the DSP at 8 kHz is accumulated.
V_{FS}, I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.

VARTHR register is an 8-bit unsigned number, so its maximum value is $2^8 - 1$. Its default value is 0x3. Values lower than 3, that is 2 or 1 should be avoided and 0 should never be used as the threshold must be a non-zero value.

This discrete time accumulation or summation is equivalent to integration in continuous time following the expression in Equation (39):

$$ReactiveEnergy = \int q(t)dt = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} q(nT) \times T \right\} \quad (39)$$

where:
n is the discrete time sample number.
T is the sample period.

On the ADE7978, the total phase reactive powers are accumulated in the AVARHR, BVARHR, and CVARHR 32-bit signed registers. The fundamental phase reactive powers are accumulated in the AFVARHR, BFVARHR, and CFVARHR 32-bit signed registers. The reactive energy register content can roll over to full-scale negative (0x80000000) and continue increasing in value when the reactive power is positive. Conversely, if the reactive power is negative, the energy register underflows to full-scale positive (0x7FFFFFFF) and continues to decrease in value.

Bit 2 (REHF) in the STATUS0 register is set when Bit 30 of one of the xVARHR registers changes, signifying one of these registers is half full. If the reactive power is positive, the var-hour register becomes half full when it increments from 0x3FFF FFFF to 0x4000 0000. If the reactive power is negative, the var-hour register becomes half full when it decrements from 0xC000 0000 to 0xBFFF FFFF. Analogously, Bit 3 (FREHF) in the STATUS0 register is set when Bit 30 of one of the xFVARHR registers changes, signifying one of these registers is half full.

Setting Bits[3:2] in the MASK0 register enable the FREHF and REHF interrupts, respectively. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever one of the energy registers, xVARHR (for REHF interrupt) or xFVARHR (for FREHF interrupt), becomes half full. The status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to high by writing to the STATUS0 register with the corresponding bit set to 1.

Setting Bit 6 (RSTREAD) of the LCYCMODE register enables a read-with-reset for all var-hour accumulation registers, that is, the registers are reset to 0 after a read operation.

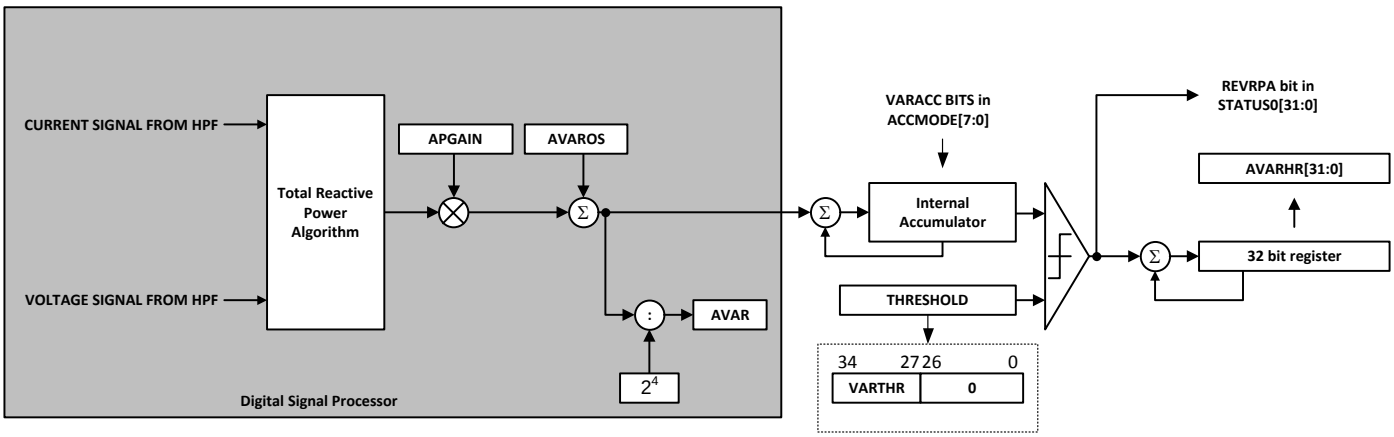


Figure 64. Total Reactive Energy Accumulation

Integration Time Under A Steady Load

The discrete time sample period (T) for the accumulation register is 976.5625 ns (1.024 MHz frequency). With full-scale sinusoidal signals on the analog inputs and a 90° phase difference between the voltage and the current signal (the largest possible reactive power), the average word value representing the reactive power is PMAX = 26,991,271. If the VARTHR threshold is set at 3, its minimum recommended value, the first stage accumulator generates a pulse that is added to var-hour registers every

$$\frac{3\times 2^{27}}{PMAX\times 1.024\times 10^{6}} = 14.5683\mu\text{sec}$$

The maximum value that can be stored in the var-hour accumulation register before it overflows is $2^{31} - 1$ or 0x7FFFFFFF. The integration time is calculated as

$$Time = 0\text{x}7\text{FFF,FFFF} \times 14.5683\ \mu\text{s} = 8\ \text{hr}\ 41\ \text{min}\ 25\text{sec} \quad (40)$$

Energy Accumulation Modes

The reactive power accumulated in each var-hour accumulation 32-bit register (AVARHR, BVARHR, CVARHR, AFVARHR, BFVARHR, and CFVARHR) depends on the configuration of Bits[5:4] (CONSEL[1:0]) in the ACCMODE register, in correlation with the watt-hour registers. The different configurations are described in Table 24. Note that IA′/IB′/IC′ are the phase-shifted current waveforms.

Table 24. Inputs to Var-Hour Accumulation Registers

CONSEL[1:0]	AVARHR, AFVARHR	BVARHR, BFVARHR	CVARHR, CFVARHR
00	VA × IA′	VB × IB′	VC × IC′
01	VA × IA′	VB × IB′ VB=VA-VC[1]	VC × IC′
10	VA × IA′	VB × IB′ VB = –VA – VC	VC × IC′
11	VA × IA′	VB × IB′ VB = –VA	VC × IC′

[1] In a 3-phase three wire case (CONSEL[1:0] = 01), the ADE7978 computes the rms value of the line voltage between phases A and C and stores the result into BVRMS register (see the Voltage RMS in 3-Phase Three Wire Delta Configurations section). The Phase B current determined after the HPF is 0. Consequently, the powers associated with Phase B are 0. To avoid any errors in the frequency output pins (CF1, CF2, or CF3) related to the powers associated with Phase B, disable the contribution of Phase B to the energy-to-frequency converters by setting bits TEMSEL1[1] or TERMSEL2[1] or TERMSEL3[1] to 0 in the COMPMODE register (see the Energy-to-Frequency Conversion section).

Bits[3:2] (VARACC[1:0]) in the ACCMODE register determine how the reactive power is accumulated in the var-hour registers and how the CF frequency output can be generated function of total and fundamental active and reactive powers. See the Energy-to-Frequency Conversion section for details.

Line Cycle Reactive Energy Accumulation Mode

As mentioned in the Line Cycle Active Energy Accumulation Mode section, in line cycle energy accumulation mode, the energy accumulation can be synchronized to the voltage channel zero crossings so that reactive energy can be accumulated over an integral number of half line cycles.

In this mode, the ADE7978 transfers the reactive energy accumulated in the 32-bit internal accumulation registers into the xVARHR or xFVARHR registers after an integral number of line cycles, as shown in Figure 65. The number of half line cycles is specified in the LINECYC register.

The line cycle reactive energy accumulation mode is activated by setting Bit 1 (LVAR) in the LCYCMODE register. The total reactive energy accumulated over an integer number of half line cycles or zero crossings is available in the var-hour accumulation registers after the number of zero crossings specified in the LINECYC register is detected. When using the line cycle accumulation mode, the Bit 6 (RSTREAD) of the LCYCMODE register should be set to Logic 0 because a read with reset of var-hour registers outside the LINECYC period resets the energy accumulation.

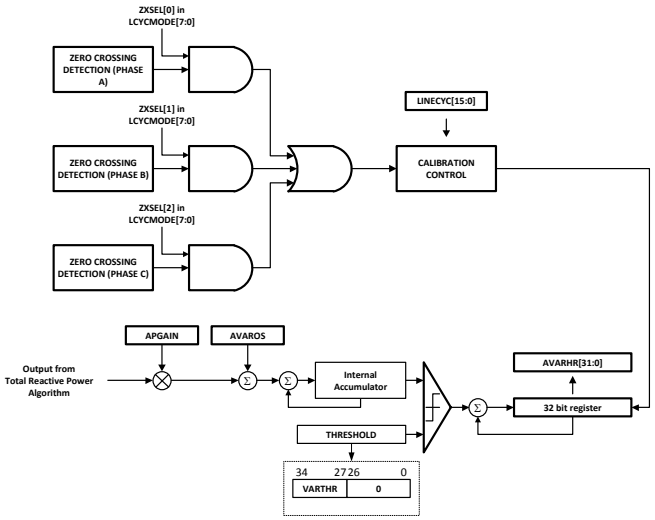


Figure 65. Line Cycle Total Reactive Energy Accumulation Mode

Phase A, Phase B, and Phase C zero crossings are, respectively, included when counting the number of half line cycles by setting Bits[5:3] (ZXSEL[x]) in the LCYCMODE register. Any combination of the zero crossings from all three phases can be used for counting the zero crossing. Select only one phase at a time for inclusion in the zero-crossings count during calibration.

For details on setting the LINECYC register and the Bit 5 (LENERGY) in the MASK0 interrupt mask register associated with the line cycle accumulation mode, see the Line Cycle Active Energy Accumulation Mode section.

APPARENT POWER CALCULATION

Apparent power is defined as the maximum active power that can be delivered to a load. One way to obtain the apparent power is by multiplying the voltage rms value by the current rms value (also called the arithmetic apparent power).

$$S = V\ rms \times I\ rms \quad (41)$$

where:
S is the apparent power.
V rms and *I rms* are the rms voltage and current, respectively.

The ADE7978 computes the arithmetic apparent power on each phase. Figure 66 illustrates the signal processing in each phase for the calculation of the apparent power in the ADE7978. Because V rms and I rms contain all harmonic information, the apparent power computed by the ADE7978 is total apparent power. The ADE7978 does not compute the fundamental apparent power.

The ADE7978 stores the instantaneous phase apparent powers into the AVA, BVA, and CVA registers. Their equation is

$$xVA = \frac{V}{V_{FS}} \times \frac{I}{I_{FS}} \times PMAX \times \frac{1}{2^4} \quad (42)$$

where:
V, I are the rms values of the phase voltage and current.
V_{FS}, I_{FS} are the rms values of the phase voltage and current when the ADC inputs are at full scale.
PMAX = 26,991,271, the instantaneous power computed when the ADC inputs are at full scale and in phase.

The xVA[23:0] waveform registers may be accessed using various serial ports. Refer to the Waveform Sampling Mode section for more details.

The ADE7978 can compute the apparent power in an alternative way by multiplying the phase rms current by an rms voltage introduced externally. See the Apparent Power Calculation Using VNOM section for details.

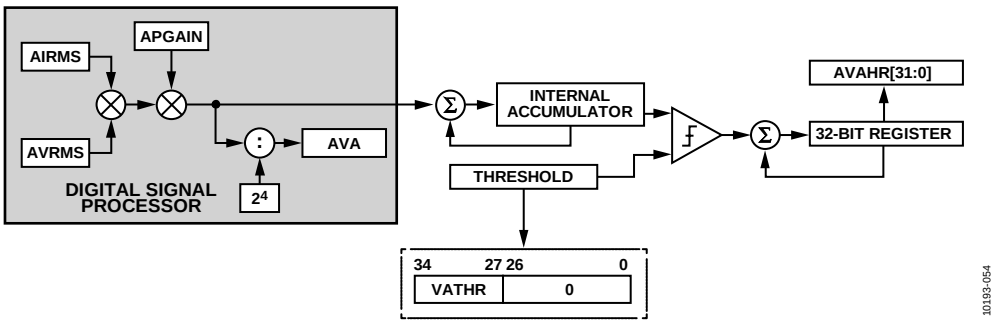


Figure 66. Apparent Power Data Flow and Apparent Energy Accumulation

Apparent Power Gain Calibration

The average apparent power result in each phase can be scaled by ±100% by writing to one of the phase's PGAIN 24-bit registers (APGAIN, BPGAIN, or CPGAIN). Note that these registers are the same gain registers used to compensate the other powers computed by the ADE7978. See the Active Power Gain Calibration section for details on these registers.

Apparent Power Offset Calibration

Each rms measurement includes an offset compensation register to calibrate and eliminate the dc component in the rms value (see the Root Mean Square Measurement section). The voltage and current rms values are multiplied together in the apparent power signal processing. As no additional offsets are created in the multiplication of the rms values, there is no specific offset compensation in the apparent power signal processing. The offset compensation of the apparent power measurement in each phase is accomplished by calibrating each individual rms measurement.

Apparent Power Calculation Using VNOM

The ADE7978 can compute the apparent power by multiplying the phase rms current by an rms voltage introduced externally in the VNOM 24-bit signed register.

When one of Bits[13:11] (VNOMCEN, VNOMBEN, or VNOMAEN) in the COMPMODE register is set to 1, the apparent power in the corresponding phase (Phase x for VNOMxEN) is computed in this way. When the VNOMxEN bits are cleared to 0, the default value, then the arithmetic apparent power is computed.

The VNOM register contains a number determined by V, the nominal phase rms voltage, and V_{FS}, the rms value of the phase voltage when the ADC inputs are at full scale:

$$VNOM = \frac{V}{V_{FS}} \times 3{,}761{,}808 \quad (43)$$

As stated in the Current Waveform Gain Registers, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words. Similar to the register presented in Figure 47, the VNOM 24-bit signed register is accessed as a 32-bit register with the eight MSBs padded with 0s.

Apparent Energy Calculation

Apparent energy is defined as the integral of apparent power.

$$Apparent\ Energy = \int s(t)dt \quad (44)$$

Similar to active and reactive powers, the ADE7978 achieves the integration of the apparent power signal in two stages (see Figure 66). The first stage accumulates the instantaneous

apparent power at 1.024 MHz, although they are computed by the DSP at 8 kHz rate. Every time a threshold is reached, a pulse is generated and the threshold is subtracted from the internal register. The second stage consists in accumulating the pulses generated after the first stage into internal 32-bit accumulation registers. The content of these registers is transferred to the VA-hour registers, xVAHR, when these registers are accessed.

Figure 66 illustrates this process. The threshold is formed by the VATHR 8-bit unsigned register concatenated to 27 bits equal to 0. It is introduced by the user and is common for all phase total active and fundamental powers. Its value depends on how much energy is assigned to one LSB of VA-hour registers. When a derivative of apparent energy (VAh) [10^n VAh], where n is an integer, is desired as one LSB of the xVAHR register, the xVATHR register can be computed using the following equation:

$$VATHR = \frac{PMAX \times f_s \times 3600 \times 10^n}{V_{FS} \times I_{FS} \times 2^{27}} \quad (45)$$

where:
PMAX = 26,991,271, the instantaneous power computed when the ADC inputs are at full scale.
f_S = 1.024 MHz, the frequency at which every instantaneous power computed by the DSP at 8 kHz is accumulated.
V_{FS}, I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.

The VATHR register is an 8-bit unsigned number, so its maximum value is $2^8 - 1$. Its default value is 0x3. Values lower than 3, that is 2 or 1 should be avoided and 0 should never be used as the threshold must be a non-zero value.

This discrete time accumulation or summation is equivalent to integration in continuous time following the description in Equation (46).

$$ApparentEnergy = \int s(t)dt = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} s(nT) \times T \right\} \quad (46)$$

where:
n is the discrete time sample number.
T is the sample period.

In the ADE7978, the phase apparent powers are accumulated in the AVAHR, BVAHR, and CVAHR 32-bit signed registers. The apparent energy register content can roll over to full-scale negative (0x80000000) and continue increasing in value when the apparent power is positive.

The ADE7978 provides a status flag to signal when one of the xVAHR registers is half full. Bit 4 (VAEHF) in the STATUS0 register is set when Bit 30 of one of the xVAHR registers changes, signifying one of these registers is half full. As the apparent power is always positive and the xVAHR registers are signed, the VA-hour registers become half full when they increment from 0x3FFFFFFF to 0x40000000. Interrupts attached to Bit VAEHF in the STATUS0 register can be enabled by setting Bit 4 in the MASK0 register. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever one of the Energy Registers xVAHR becomes half full. The status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to high by writing to the STATUS0 register with the corresponding bit set to 1.

Setting Bit 6 (RSTREAD) of the LCYCMODE register enables a read-with-reset for all xVAHR accumulation registers, that is, the registers are reset to 0 after a read operation.

Integration Time Under Steady Load

The discrete time sample period for the accumulation register is 976.5625 ns (1.024 MHz frequency). With full-scale pure sinusoidal signals on the analog inputs, the average word value representing the apparent power is PMAX. If the VATHR threshold register is set at 3, its minimum recommended value, the first stage accumulator generates a pulse that is added to the xVAHR registers every $\frac{3 \times 2^{27}}{PMAX \times 1.024 \times 10^6} = 14.5683 \mu\text{sec}$

The maximum value that can be stored in the xVAHR accumulation register before it overflows is $2^{31} - 1$ or 0x7FFFFFFF. The integration time is calculated as

$$Time = 0\text{x}7FFFFFFF \times 14.5683\ \mu\text{s} = 8\ \text{hr}\ 41\ \text{min}\ 25\ \text{sec} \quad (47)$$

Energy Accumulation Mode

The apparent power accumulated in each accumulation register depends on the configuration of Bits[5:4] (CONSEL[1:0]) in the ACCMODE register. The various configurations are described in Table 25.

Table 25. Inputs to VA-Hour Accumulation Registers

CONSEL[1:0]	AVAHR	BVAHR	CVAHR
00	AVRMS × AIRMS	BVRMS × BIRMS	CVRMS × CIRMS
01	AVRMS × AIRMS	BVRMS × BIRMS VB = VA – VC[1]	CVRMS × CIRMS
10	AVRMS × AIRMS	BVRMS × BIRMS VB = –VA – VC	CVRMS × CIRMS
11	AVRMS × AIRMS	BVRMS × BIRMS VB = –VA	CVRMS × CIRMS

[1] In a 3-phase three wire case (CONSEL[1:0] = 01), the ADE7978 computes the rms value of the line voltage between Phase A and Phase C and stores the result into the BVRMS register (see the Voltage RMS in 3-Phase Three Wire Delta Configurations section). The Phase B current determined after the HPF is 0. Consequently, the powers associated with Phase B are 0. To avoid any errors in the frequency output pins (CF1, CF2, or CF3) related to the powers associated with Phase B, disable the contribution of Phase B to the energy-to-frequency converters by setting bits TEMSEL1[1] or TERMSEL2[1] or TERMSEL3[1] to 0 in the COMPMODE register (see the Energy-to-Frequency Conversion section).

Line Cycle Apparent Energy Accumulation Mode

As described in the Line Cycle Active Energy Accumulation Mode section, in line cycle energy accumulation mode, the energy accumulation can be synchronized to the voltage channel zero crossings allowing apparent energy to be accumulated over an integral number of half line cycles. In this mode, the ADE7978 transfers the apparent energy accumulated in the 32-bit internal accumulation registers into the xVAHR registers after an

integral number of line cycles, as shown in Figure 67. The number of half line cycles is specified in the LINECYC register.

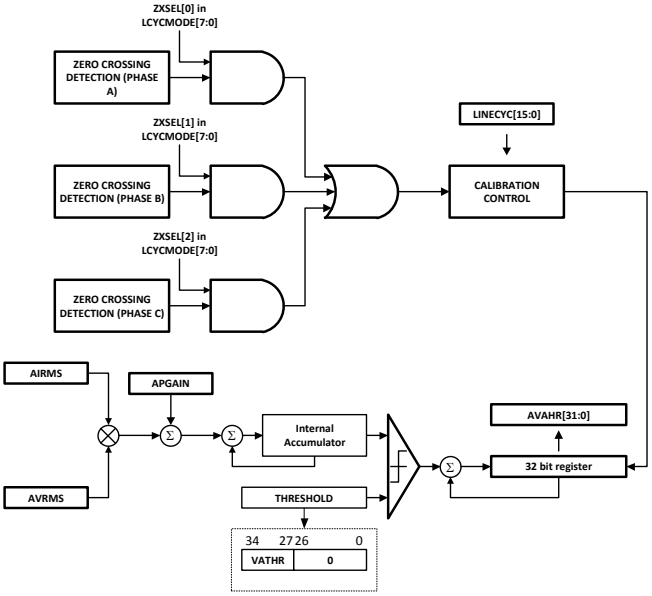


Figure 67. Line Cycle Apparent Energy Accumulation Mode

The line cycle apparent energy accumulation mode is activated by setting Bit 2 (LVA) in the LCYCMODE register. The apparent energy accumulated over an integer number of zero crossings is written to the xVAHR accumulation registers after the number of zero crossings specified in LINECYC register is detected. When using the line cycle accumulation mode, the Bit 6 (RSTREAD) of the LCYCMODE register should be set to Logic 0 because a read with reset of xVAHR registers outside the LINECYC period resets the energy accumulation.

Phase A, Phase B, and Phase C zero crossings are, respectively, included when counting the number of half line cycles by setting Bits[5:3] (ZXSEL[x]) in the LCYCMODE register. Any combination of the zero crossings from all three phases can be used for counting the zero crossing. Select only one phase at a time for inclusion in the zero-crossings count during calibration.

For details on setting the LINECYC register and Bit 5 (LENERGY) in the MASK0 interrupt mask register associated with the line cycle accumulation mode, see the Line Cycle Active Energy Accumulation Mode section.

POWER FACTOR CALCULATION

The ADE7978 provides a direct power factor measurement simultaneously on all phases. Power factor in an ac circuit is defined as the ratio of the total active power flowing to the load to the apparent power. The absolute power factor measurement is defined in terms of leading or lagging referring to whether the current is leading or lagging the voltage waveform. When the current is leading the voltage, the load is capacitive and this is defined as a negative power factor. When the current is lagging the voltage, the load is inductive and this is defined as a positive power factor. The relationship of the current to the voltage waveform is illustrated in Figure 68.

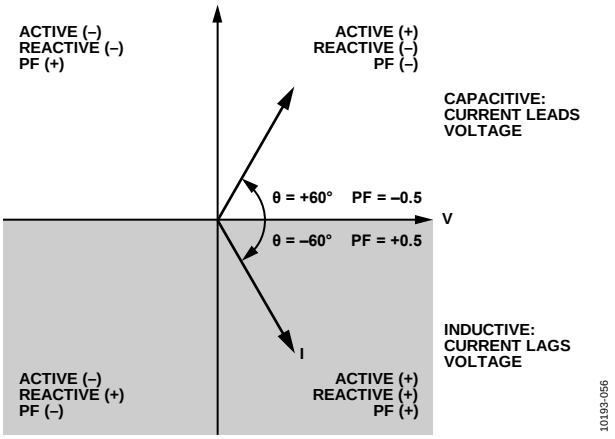


Figure 68. Capacitive and Inductive Loads

As shown in Figure 68, the reactive power measurement is negative when the load is capacitive, and positive when the load is inductive. The sign of the reactive power can therefore be used to reflect the sign of the power factor. The ADE7978 uses the sign of the total reactive power as the sign of the absolute power factor. If the total reactive power is in no load state, then the sign of the power factor is the sign of the total active power.

The mathematical definition of power factor is shown in Equation (48):

$$Power\ Factor = (Sign\ Total\ Reactive\ Power) \times \frac{Total\ Active\ Power}{Apparent\ Power} \quad (48)$$

As previously mentioned, the ADE7978 provides a power factor measurement on all phases simultaneously. These readings are provided into three 16-bit signed registers, APF (Address 0xE902) for Phase A, BPF (Address 0xE903) for Phase B, and CPF (Address 0xE904) for Phase C. The registers are signed twos complement register with the MSB indicating the polarity of the power factor. Each LSB of the APF, BPF, and CPF registers equates to a weight of 2^{-15}, hence the maximum register value of 0x7FFF equating to a power factor value of 1. The minimum register value of 0x8000 corresponds to a power factor of −1. If because of offset and gain calibrations, the power factor is outside the −1 to +1 range, the result is set at −1 or +1 depending on the sign of the fundamental reactive power.

By default, the instantaneous total phase active and apparent powers are used to calculate the power factor and the registers are updated at a rate of 8 kHz. The sign bit is taken from the instantaneous total phase reactive energy measurement on each phase.

Should a measurement with more averaging be required, the ADE7978 provides an option of using the line cycle accumulation measurement on the active and apparent energies to determine the power factor. This option provides a more stable power factor reading. This mode is enabled by setting the PFMODE bit (Bit 7) in the LCYCMODE register (Address 0xE702). When this mode is enabled the line cycle accumulation mode must be

enabled on both the active and apparent energies. This is done by setting the xLWATT and xLVA bits in the LCYCMODE register (Address 0xE702). The update rate of the power factor measurement is now an integral number of half line cycles that can be programmed into the LINECYC register (Address 0xE60C). For full details on setting up the line cycle accumulation mode see the Line Cycle Active Energy Accumulation Mode, Line Cycle Reactive Energy Accumulation Mode, and Line Cycle Apparent Energy Accumulation Mode sections.

Note that the power factor measurement is effected by the no load condition if it is enabled (see the No Load Condition section). If the apparent energy no load is true, then the power factor measurement is set to 1. If the no load condition based on total active and reactive energies is true, the power factor measurement is set at 0.

TOTAL HARMONIC DISTORTION CALCULATION

The ADE7978 computes the total harmonic distortion (THD) on all phase currents and voltages. The THD expressions are shown in Equations (49):

$$THD_I = \frac{\sqrt{I^2 - I_1^2}}{I_1}$$
$$THD_V = \frac{\sqrt{V^2 - V_1^2}}{V_1} \quad (49)$$

Where: I and V are the rms values of the phase currents and voltages stored into AIRMS, AVRMS, BIRMS, BVRMS, CIRMS, and CVRMS registers. I_1 and V_1 are the fundamental rms values stored into AFIRMS, AFVRMS, BFIRMS, BFVRMS, CFIRMS, and CFVRMS registers.

The THD calculations are stored into AITHD, BITHD, CITHD, AVTHD. BVTHD, and CVTHD registers. They are 24-bit registers in 3.21 signed format. This means the ratios are limited to +3.9999 and all greater results are clamped to it.

Similar to the registers presented in Figure 55, the THD 24-bit registers are transmitted as 32-bit registers with the eight MSBs padded with 0s.

WAVEFORM SAMPLING MODE

The waveform samples of the current and voltage waveform, the active, reactive, and apparent power outputs, the total harmonic distortions are stored every 125 μs (8 kHz rate) into 24-bit signed registers that can be accessed through various serial ports of the ADE7978. Table 26 provides a list of registers and their descriptions.

Table 26. Waveform Registers List

Register	Description
IAWV	Phase A current
IBWV	Phase B current
ICWV	Phase C current
INWV	Neutral current
VAWV	Phase A voltage
VBWV	Phase B voltage
VCWV	Phase C voltage
VA2WV	Phase A auxiliary voltage
VB2WV	Phase B auxiliary voltage
VC2WV	Phase C auxiliary voltage
VNWV	Neutral line voltage
VN2WV	Neutral line auxiliary voltage
AVA	Phase A apparent power
BVA	Phase B apparent power
CVA	Phase C apparent power
AWATT	Phase A total active power
BWATT	Phase B total active power
CWATT	Phase C total active power
AVAR	Phase A total reactive power
BVAR	Phase B total reactive power
CVAR	Phase C total reactive power
AVTHD	Phase A voltage total harmonic distortion
AITHD	Phase A current total harmonic distortion
BVTHD	Phase B voltage total harmonic distortion
BITHD	Phase B current total harmonic distortion
CVTHD	Phase C voltage total harmonic distortion
CITHD	Phase C current total harmonic distortion

Bit 17 (DREADY) in the STATUS0 register can be used to signal when the registers listed in Table 26 can be read using I²C or SPI serial ports. An interrupt attached to the flag can be enabled by setting Bit 17 (DREADY) in the MASK0 register. (see the Digital Signal Processor section for more details on Bit DREADY). Additionally, the ZX/$\overline{\text{DREADY}}$ pin goes low 6.5μs before bit DREADY is set to 1. It stays low for 10μs and then goes back high. This happens when bits 1,0 (ZX_DREADY) in the CONFIG register are set to 00. The $\overline{\text{DREADY}}$ functionality at the ZX/$\overline{\text{DREADY}}$ pin may be used to initiate a burst read of the waveform sample registers. See I²C Burst Read Operation and SPI Burst Read Operation sections for details.

The ADE7978 contains a high speed data capture (HSDC) port that is specially designed to provide fast access to the following waveform sample registers: IAWV, IBWV, ICWV, INWV, VAWV, VBWV, VCWV, AWATT, BWATT, CWATT, AVAR, BVAR, CVAR, AVA, BVA and CVA. Read the HSDC Interface section for more details.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7978 work on 32-, 16-, or 8-bit words. All registers listed in Table 26 are transmitted signed extended from 24 bits to 32 bits (see Figure 34).

ENERGY-TO-FREQUENCY CONVERSION

The ADE7978 provides three frequency output pins: CF1, CF2, and CF3. The CF3 pin is multiplexed with the HSCLK pin of the HSDC interface. When HSDC is enabled, the CF3 functionality is disabled at the pin. CF1 and CF2 pins are always available. After initial calibration at manufacturing, the

manufacturer or end customer verifies the energy meter calibration. One convenient way to verify the meter calibration is to provide an output frequency proportional to the active, reactive, or apparent powers under steady load conditions. This output frequency can provide a simple, single-wire, optically isolated interface to external calibration equipment. Figure 69 illustrates the energy-to-frequency conversion in the ADE7978.

The DSP computes the instantaneous values of all phase powers: total active, fundamental active, total reactive, fundamental reactive, and apparent. The process in which the energy is sign accumulated in various xWATTHR, xVARHR, and xVAHR registers has already been described in the energy calculation sections: Active Energy Calculation, Reactive Energy Calculation, and Apparent Energy Calculation. In the energy-to-frequency conversion process, the instantaneous powers generate signals at the frequency output pins (CF1, CF2, and CF3). One digital-to-frequency converter is used for every CFx pin. Every converter sums certain phase powers and generates a signal proportional to the sum. Two sets of bits decide what powers are converted.

First, Bits[2:0] (TERMSEL1[2:0]), Bits[5:3] (TERMSEL2[2:0]), and Bits[8:6] (TERMSEL3[2:0]) of the COMPMODE register decide which phases, or which combination of phases, are added.

The TERMSEL1 bits refer to the CF1 pin, the TERMSEL2 bits refer to the CF2 pin, and the TERMSEL3 bits refer to the CF3 pin. The TERMSELx[0] bits manage Phase A. When set to 1, Phase A power is included in the sum of powers at the CFx converter. When cleared to 0, Phase A power is not included. The TERMSELx[1] bits manage Phase B, and the TERMSELx[2] bits manage Phase C. Setting all TERMSELx bits to 1 means all 3-phase powers are added at the CFx converter. Clearing all TERMSELx bits to 0 means no phase power is added and no CF pulse is generated.

Second, Bits[2:0] (CF1SEL[2:0]), Bits[5:3] (CF2SEL[2:0]), and Bits[8:6] (CF3SEL[2:0]) in the CFMODE register decide what type of power is used at the inputs of the CF1, CF2, and CF3 converters, respectively. Table 27 shows the values that CFxSEL can have: total active, total reactive, apparent, fundamental active, or fundamental reactive powers.

Table 27. CFxSEL Bits Description

CFxSEL	Description	Registers Latched When CFxLATCH = 1
000	CFx signal proportional to the sum of total phase active powers	AWATTHR, BWATTHR, CWATTHR
001	CFx signal proportional to the sum of total phase reactive powers	AVARHR, BVARHR, CVARHR
010	CFx signal proportional to the sum of phase apparent powers	AVAHR, BVAHR, CVAHR
011	CFx signal proportional to the sum of fundamental phase active powers	AFWATTHR, BFWATTHR, CFWATTHR
100	CFx signal proportional to the sum of fundamental phase reactive powers	AFVARHR, BFVARHR, CFVARHR
101 to 111	Reserved	

By default, the TERMSELx bits are all 1 and the CF1SEL bits are 000, the CF2SEL bits are 001, and the CF3SEL bits are 010. This means that by default, the CF1 digital-to-frequency converter produces signals proportional to the sum of all 3-phase total active powers, CF2 produces signals proportional to total reactive powers, and CF3 produces signals proportional to apparent powers.

Similar to the energy accumulation process, the energy-to-frequency conversion is accomplished in two stages. The first stage is the same stage illustrated in the energy accumulation sections of active, reactive and apparent powers (see Active Energy Calculation, Reactive Energy Calculation, Apparent Energy Calculation sections). The second stage consists of the frequency divider by the CFxDEN 16-bit unsigned registers. The values of CFxDEN depend on the meter constant (MC), measured in impulses/kWh and how much energy is assigned to one LSB of various energy registers: xWATTHR, xVARHR, and so forth. Suppose a derivative of Wh [10^n Wh] where n is a positive or negative integer, is desired as one LSB of xWATTHR register. Then, CFxDEN is as follows:

$$CFxDEN = \frac{10^3}{MC[\text{imp/kwh}] \times 10^n} \quad (50)$$

The derivative of wh must be chosen in such a way to obtain a CFxDEN register content greater than 1. If CFxDEN = 1, then the CFx pin stays active low for only 1 µs. Thus, CFxDEN register should not be set to 1. The frequency converter cannot accommodate fractional results; the result of the division must be rounded to the nearest integer. If CFxDEN is set equal to 0, then the ADE7978 considers it to be equal to 1.

The CFx pulse output stays low for 80 ms if the pulse period is larger than 160 ms (6.25 Hz). If the pulse period is smaller than 160 ms and CFxDEN is an even number, the duty cycle of the pulse output is exactly 50%. If the pulse period is smaller than 160 ms and CFxDEN is an odd number, the duty cycle of the pulse output is

$$(1+1/CFxDEN) \times 50\%$$

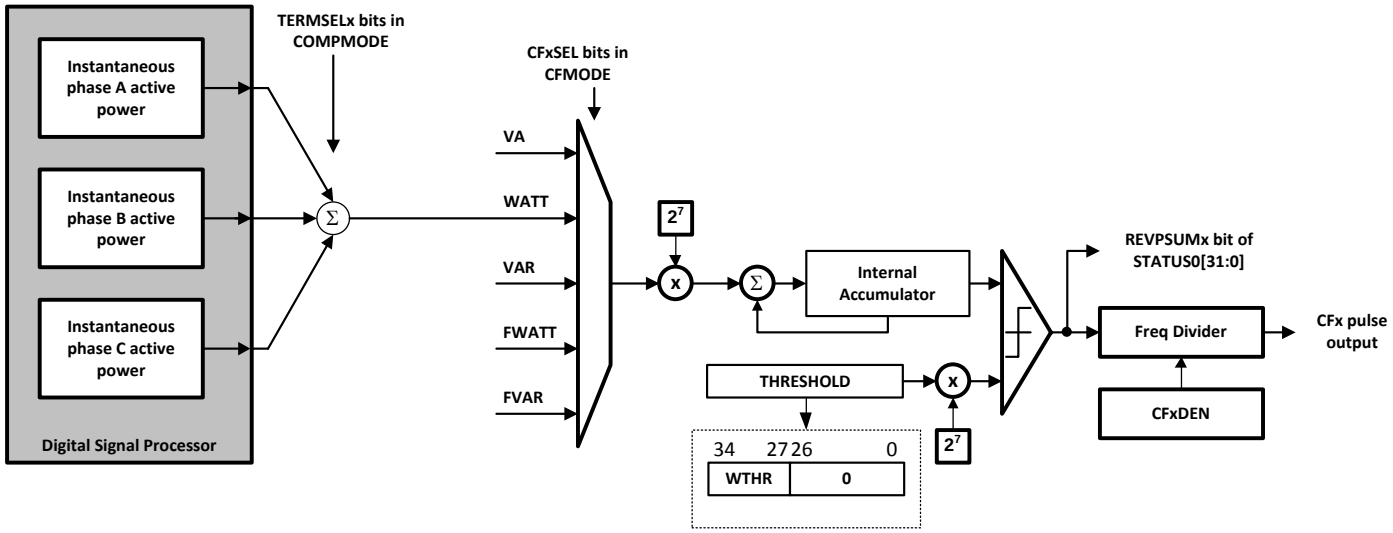


Figure 69. Energy-to-Frequency Conversion

The CFx pulse output is active low and preferably connected to an LED, as shown in Figure 70. No transistor is required to supplement the drive strength of the CFx pin.

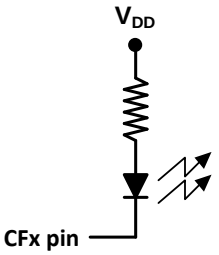


Figure 70. CFx Pin Recommended Connection

Bits[11:9] (CF3DIS, CF2DIS, and CF1DIS) of the CFMODE register decide if the frequency converter output is generated at the CF3, CF2, or CF1 pin. When Bit CFxDIS is set to 1 (the default value), the CFx pin is disabled and the pin stays high. When Bit CFxDIS is cleared to 0, the corresponding CFx pin output generates an active low signal.

Bits[16:14] (CF3, CF2, CF1) in the Interrupt Mask register MASK0 manage the CF3, CF2, and CF1 related interrupts. When the CFx bits are set, whenever a high-to-low transition at the corresponding frequency converter output occurs, an interrupt $\overline{\text{IRQ0}}$ is triggered and a status bit in the STATUS0 register is set to 1. The interrupt is available even if the CFx output is not enabled by the CFxDIS bits in the CFMODE register.

Synchronizing Energy Registers with CFx Outputs

The ADE7978 contains a feature that allows synchronizing the content of phase energy accumulation registers with the generation of a CFx pulse. When a high-to-low transition at one frequency converter output occurs, the content of all internal phase energy registers that relate to the power being output at CFx pin is latched into hour registers and then resets to 0. See Table 27 for the list of registers that are latched based on the CFxSEL[2:0] bits in the CFMODE register. All 3-phase registers are latched independent of the TERMSELx bits of the COMPMODE register. The process is shown in Figure 71 for CF1SEL[2:0] = 010 (apparent powers contribute at the CF1 pin) and CFCYC = 2.

The CFCYC 8-bit unsigned register contains the number of high to low transitions at the frequency converter output between two consecutive latches. Avoid writing a new value into the CFCYC register during a high-to-low transition at any CFx pin.

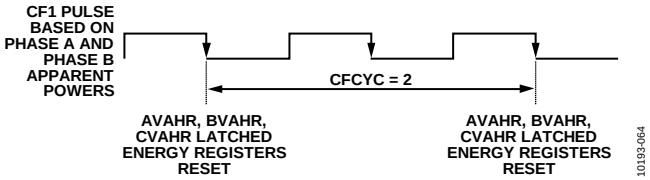


Figure 71. Synchronizing AVAHR and BVAHR with CF1

Bits[14:12] (CF3LATCH, CF2LATCH, and CF1LATCH) of the CFMODE register enable this process when set to 1. When cleared to 0, the default state, no latch occurs. The process is available even if the CFx output is not enabled by the CFxDIS bits in the CFMODE register.

Energy Registers and CF Outputs for Various Accumulation Modes

Bits[1:0] (WATTACC[1:0]) in the ACCMODE register determine the accumulation modes of the total and fundamental active powers when signals proportional to the active powers are chosen at the CFx pins (the CFxSEL[2:0] bits in the CFMODE register equal 000 or 011). They also determine the accumulation modes of the watt-hour energy registers (AWATTHR, BWATTHR, CWATTHR, AFWATTHR, BFWATTHR and CFWATTHR). When WATTACC[1:0] = 00 (the default value), the active powers are sign accumulated in the watt-hour registers and before entering the energy-to-frequency converter. Figure 72 shows how signed active power accumulation works. In this mode, the CFx pulses

synchronize perfectly with the active energy accumulated in xWATTHR registers because the powers are sign accumulated in both data paths.

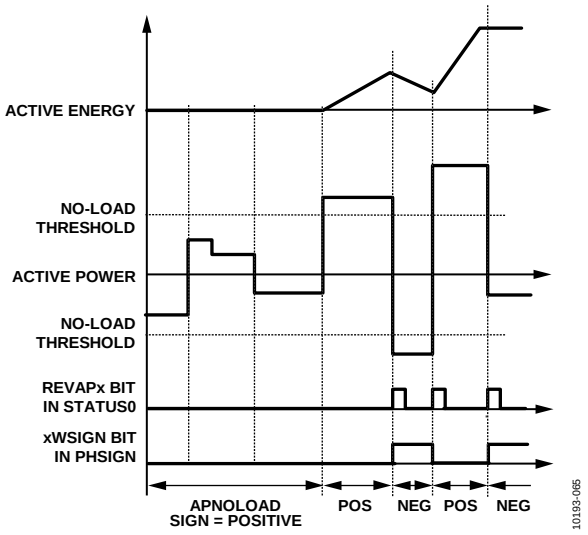


Figure 72. Active Power Signed Accumulation Mode

When WATTACC[1:0] = 01, the active powers are accumulated in positive only mode. When the powers are negative, the watt-hour energy registers are not accumulated. CFx pulses are generated based on signed accumulation mode. In this mode, the CFx pulses do not synchronize perfectly with the active energy accumulated in xWATTHR and xFWATTHR registers because the powers are accumulated differently in each data path. Figure 73 shows how positive only active power accumulation works.

WATTACC[1:0] = 10 setting is reserved and the ADE7978 behaves identically to the case when WATTACC[1:0] = 00.

When WATTACC[1:0] = 11, the active powers are accumulated in absolute mode. When the powers are negative, they change sign and accumulate together with the positive power in the watt-hour registers and before entering the energy-to-frequency converter. In this mode, the CFx pulses synchronize perfectly with the active energy accumulated in xWATTHR and xFWATTHR registers because the powers are accumulated in the same way in both data paths. Figure 74 shows how absolute active power accumulation works.

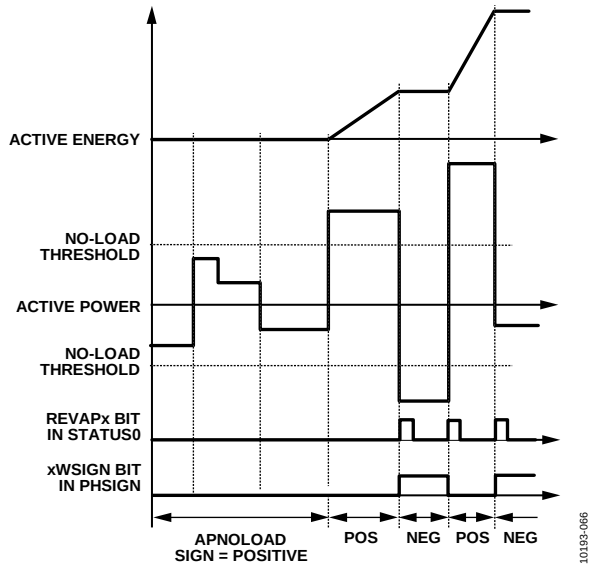


Figure 73. Active Power Positive Only Accumulation Mode

Bits[3:2] (VARACC[1:0]) in the ACCMODE register determine the accumulation modes of the total and fundamental reactive powers when signals proportional to the reactive powers are chosen at the CFx pins (the CFxSEL[2:0] bits in the CFMODE register equal 001 or 100). When VARACC[1:0] = 00, the default value, the reactive powers are sign accumulated in the var-hour energy registers and before entering the energy-to-frequency converter. Figure 75 shows how signed reactive power accumulation works. In this mode, the CFx pulses synchronize perfectly with the reactive energy accumulated in the xVARHR and xFVARHR registers because the powers are sign accumulated in both data paths.

VARACC[1:0] = 01 setting is reserved and ADE7978 behaves identically to the case when VARACC[1:0] = 00.

When VARACC[1:0] = 10, the reactive powers are accumulated depending on the sign of the corresponding active power in the var-hour energy registers and before entering the energy-to-frequency converter. If the active power is positive or considered 0 when lower than the no load threshold APNOLOAD, the reactive power is accumulated as is. If the active power is negative, the sign of the reactive power is changed for accumulation. Figure 76 shows how the sign adjusted reactive power accumulation mode works. In this mode, the CFx pulses synchronize perfectly with the reactive energy accumulated in xVARHR and xFVARHR registers because the powers are accumulated in the same way in both data paths.

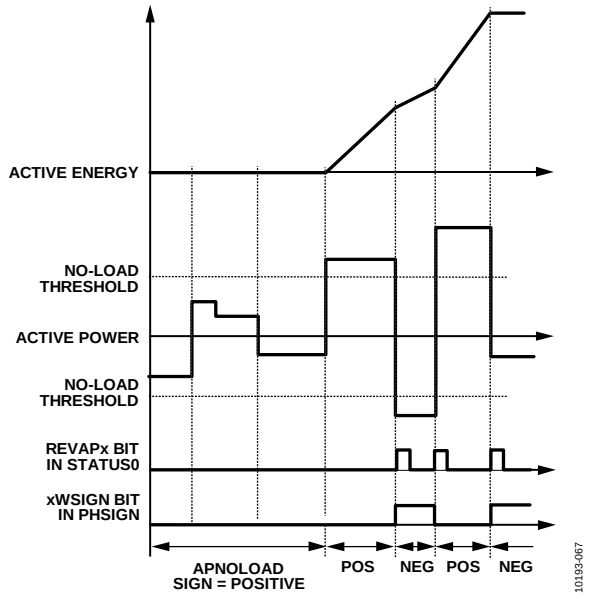


Figure 74. Active Power Absolute Accumulation Mode

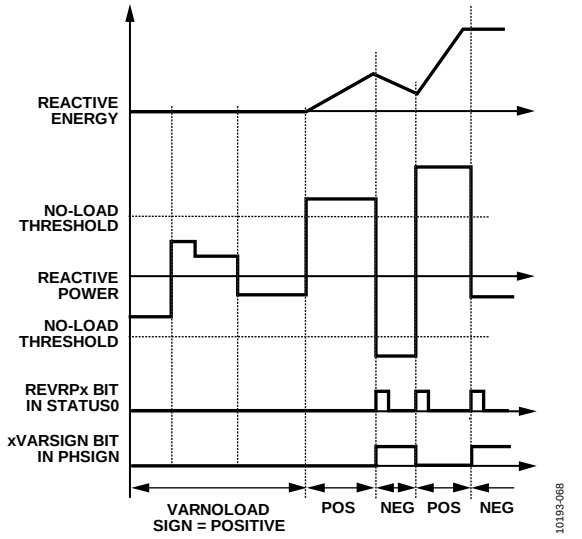


Figure 75. Reactive Power Signed Accumulation Mode

When VARACC[1:0] = 11, the reactive powers are accumulated in absolute mode. When the powers are negative, they change sign and accumulate together with the positive power in the var-hour registers and before entering the energy-to-frequency converter. In this mode, the CFx pulses synchronize perfectly with the reactive energy accumulated in xVARHR registers. Figure 77 shows how absolute reactive power accumulation works.

Sign of Sum-of-Phase Powers in the CFx Datapath

The ADE7978 has sign detection circuitry for the sum of phase powers that are used in the CFx data path. As seen in the beginning of the Energy-to-Frequency Conversion section, the energy accumulation in the CFx data path is executed in two stages. Every time a sign change is detected in the energy accumulation at the end of the first stage, that is, after the energy accumulated into the accumulator reaches one of the WTHR, VARTHR, or VATHR thresholds, a dedicated interrupt can be triggered synchronously with the corresponding CFx pulse. The sign of each sum can be read in the PHSIGN register.

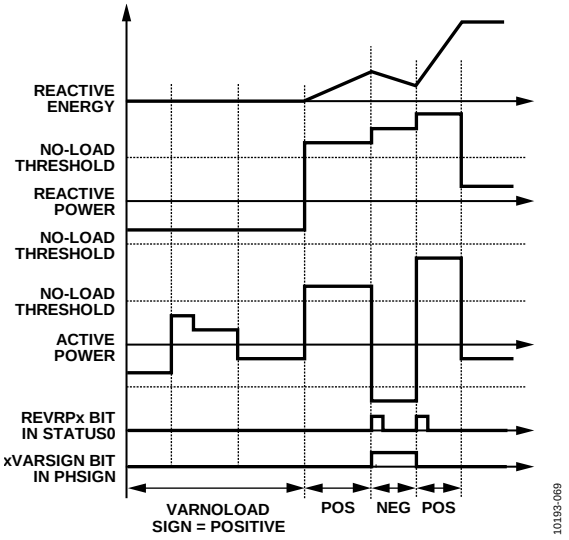


Figure 76. Reactive Power Accumulation in Sign Adjusted Mode

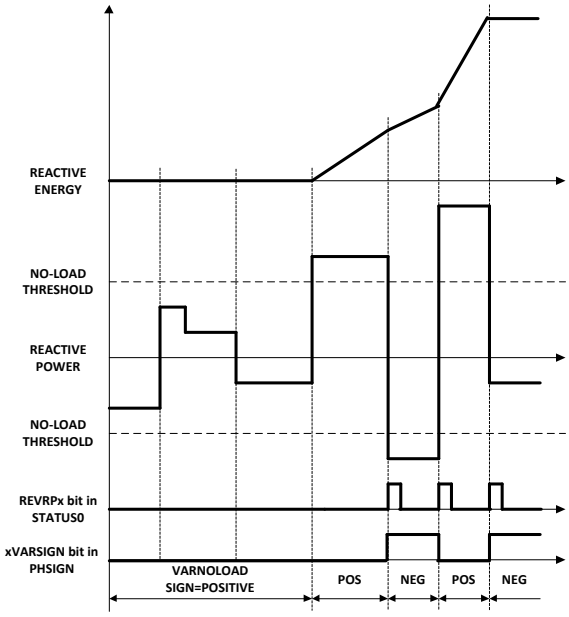


Figure 77. Reactive Power Accumulation in Absolute Mode

Bit 18, Bit 13, and Bit 9 (REVPSUM3, REVPSUM2, and REVPSUM1, respectively) of the STATUS0 register are set to 1 when a sign change of the sum of powers in CF3, CF2, or CF1 data paths occurs. To correlate these events with the pulses generated at the CFx pins, after a sign change occurs, Bit REVPSUM3, Bit REVPSUM2, and Bit REVPSUM1 are set in the same moment in which a high-to-low transition at the CF3, CF2, and CF1 pin, respectively, occurs.

Bit 8, Bit 7, and Bit 3 (SUM3SIGN, SUM2SIGN, and SUM1SIGN, respectively) of the PHSIGN register are set in the same moment with Bit REVPSUM3, Bit REVPSUM2, and Bit REVPSUM1 and indicate the sign of the sum of phase powers. When cleared to 0, the sum is positive. When set to 1, the sum is negative.

Interrupts attached to Bit 18, Bit 13, and Bit 9 (REVPSUM3, REVPSUM2, and REVPSUM1, respectively) in the STATUS0 register are enabled by setting Bit 18, Bit 13, and Bit 9 in the MASK0 register. If enabled, the $\overline{\text{IRQ0}}$ pin is set low, and the status bit is set to 1 whenever a change of sign occurs. To find the phase that triggered the interrupt, the PHSIGN register is read immediately after reading the STATUS0 register. Next, the status bit is cleared, and the $\overline{\text{IRQ0}}$ pin is set high again by writing to the STATUS0 register with the corresponding bit set to 1.

NO LOAD CONDITION

The no load condition is defined in metering equipment standards as occurring when the voltage is applied to the meter and no current flows in the current circuit. To eliminate any creep effects in the meter, the ADE7978 contains three separate no load detection circuits: one related to the total active and reactive powers, one related to the fundamental active and reactive powers, and one related to the apparent powers.

No Load Detection Based On Total Active, Reactive Powers

This no load condition is triggered when no less significant bits are accumulated into the total active and reactive energy registers on one phase (xWATTHR and xVARHR, x = A, B, or C) for a time indicated in the respective APNOLOAD and VARNOLOAD unsigned 16-bit registers. In this case, the total active and reactive energies of that phase are not accumulated and no CFx pulses are generated based on these energies.

The equations used to compute the APNOLOAD and VARNOLOAD unsigned 16-bit values are

$$APNOLOAD = 2^{16} - 1 - \frac{Y \times WTHR \times 2^{17}}{PMAX} \quad (51)$$

$$VARNOLOAD = 2^{16} - 1 - \frac{Y \times VARTHR \times 2^{17}}{PMAX}$$

where:
Y is the required no load current threshold computed relative to full scale. For example, if the no load threshold current is set 10,000 times lower than full scale value, then Y = 10,000. WTHR and VARTHR represent values stored in the WTHR and VARTHR registers and are used as the thresholds in the first stage energy accumulators for active and apparent energy, respectively (see Active Energy Calculation section). PMAX = 26,991,271, the instantaneous active power computed when the ADC inputs are at full scale.

The VARNOLOAD register usually contains the same value as the APNOLOAD register. When APNOLOAD and VARNOLOAD are set to 0x0, the no load detection circuit is disabled. If any of the APNOLOAD or VARNOLOAD thresholds is set to 0 and the other is set to a non zero value, the noload circuit is disabled and both total active and reactive powers are accumulated without any restriction.

Bit 0 (NLOAD) in the STATUS1 register is set when a no load condition in one of the three phases is triggered. Bits[2:0] (NLPHASE[2:0]) in the PHNOLOAD register indicate the state of all phases relative to a no load condition and are set simultaneously with Bit NLOAD in the STATUS1 register. NLPHASE[0] indicates the state of Phase A, NLPHASE[1] indicates the state of Phase B, and NLPHASE[2] indicates the state of Phase C. When Bit NLPHASE[x] is cleared to 0, it means the phase is out of a no load condition. When set to 1, it means the phase is in a no load condition.

An interrupt attached to Bit 0 (NLOAD) in the STATUS1 register can be enabled by setting Bit 0 in the MASK1 register. If enabled, the $\overline{\text{IRQ1}}$ pin is set to low, and the status bit is set to 1 whenever one of three phases enters or exits this no load condition. To find the phase that triggered the interrupt, the PHNOLOAD register is read immediately after reading the STATUS1 register. Next, the status bit is cleared, and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the corresponding bit set to 1.

No Load Detection Based on Fundamental Active and Reactive Powers

This no load condition is triggered when no less significant bits are accumulated into the fundamental active and reactive energy registers on one phase (xFWATTHR and xFVARHR, x = A, B, or C) for a time indicated in the respective APNOLOAD and VARNOLOAD unsigned 16-bit registers. In this case, the fundamental active and reactive energies of that phase are not accumulated and no CFx pulses are generated based on these energies. APNOLOAD and VARNOLOAD are the same no load thresholds set for the total active and reactive energies. When both APNOLOAD and VARNOLOAD are set to 0x0, the no load detection circuit is disabled. If any of the APNOLOAD or VARNOLOAD thresholds is set to 0 and the other is set to a non zero value, the noload circuit is disabled and both fundamental active and reactive powers are accumulated without any restriction.

Bit 1 (FNLOAD) in the STATUS1 register is set when this no load condition in one of the three phases is triggered. Bits[5:3] (FNLPHASE[2:0]) in the PHNOLOAD register indicate the state of all phases relative to a no load condition and are set simultaneously with Bit FNLOAD in the STATUS1 register. FNLPHASE[0] indicates the state of Phase A, FNLPHASE[1] indicates the state of Phase B, and FNLPHASE[2] indicates the state of Phase C. When Bit FNLPHASE[x] is cleared to 0, it means the phase is out of the no load condition. When set to 1, it means the phase is in a no load condition.

An interrupt attached to the Bit 1 (FNLOAD) in the STATUS1 register can be enabled by setting Bit 1 in the MASK1 register. If enabled, the $\overline{\text{IRQ1}}$ pin is set low and the status bit is set to 1 whenever one of three phases enters or exits this no load condition. To find the phase that triggered the interrupt, the PHNOLOAD register is read immediately after reading the STATUS1 register. Then the status bit is cleared and the $\overline{\text{IRQ1}}$

pin is set back high by writing to the STATUS1 register with the corresponding bit set to 1.

No Load Detection Based on Apparent Power

This no load condition is triggered when no less significant bits are accumulated into the apparent energy register on one phase (xVAHR, x = A, B, or C) for a time indicated by the VANOLOAD unsigned 16-bit register. In this case, the apparent energy of that phase is not accumulated and no CFx pulses are generated based on this energy.

The equation used to compute the VANOLOAD unsigned 16-bit value is

$$VANOLOAD = 2^{16} - 1 - \frac{Y \times VATHR \times 2^{17}}{PMAX} \quad (52)$$

where:

Y is the required no load current threshold computed relative to full scale. For example, if the no load threshold current is set 10,000 times lower than full scale value, then Y=10,000.

VATHR is the VATHR register used as the threshold of the first stage energy accumulator (see Apparent Energy Calculation section) PMAX = 26,991,271, the instantaneous apparent power computed when the ADC inputs are at full scale. When the VANOLOAD register is set to 0x0, the no load detection circuit is disabled.

Bit 2 (VANLOAD) in the STATUS1 register is set when this no load condition in one of the three phases is triggered. Bits[8:6] (VANLPHASE[2:0]) in the PHNOLOAD register indicate the state of all phases relative to a no load condition and they are set simultaneously with Bit VANLOAD in the STATUS1 register:

- Bit VANLPHASE[0] indicates the state of Phase A.
- Bit VANLPHASE[1] indicates the state of Phase B.
- Bit VANLPHASE[2] indicates the state of Phase C.

When Bit VANLPHASE[x] is cleared to 0, it means the phase is out of no load condition. When set to 1, it means the phase is in no load condition.

An interrupt attached to Bit 2 (VANLOAD) in the STATUS1 register is enabled by setting Bit 2 in the MASK1 register. If enabled, the $\overline{\text{IRQ1}}$ pin is set low and the status bit is set to 1 whenever one of three phases enters or exits this no load condition. To find the phase that triggered the interrupt, the PHNOLOAD register is read immediately after reading the STATUS1 register. Next, the status bit is cleared, and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the corresponding bit set to 1.

CHECKSUM REGISTER

The ADE7978 has a checksum 32-bit register, CHECKSUM, that ensures the configuration registers maintain their desired value.

All configuration registers of the ADE7978, together with reserved internal registers that always have the default value are covered by this register. The ADE7978 computes the cyclic redundancy check (CRC) based on the IEEE802.3 standard. The registers are introduced one-by-one into a linear feedback shift register (LFSR) based generator starting with the least significant bit (as shown in Figure 78). The 32-bit result is written in the CHECKSUM register. After power-up or a hardware/software reset, the CRC is computed on the default values of the registers giving a result equal to 0x6BF87803.

Figure 79 shows how the LFSR works: the configuration registers and the reserved internal registers form the bits [a_{2399}, a_{2398},…, a_0] used by LFSR. Bit a_0 is the least significant bit of the first register to enter LFSR; Bit a_{2399} is the most significant bit of the last register to enter LFSR. The formulas that govern LFSR are as follows:

- $b_i(0) = 1$, i = 0, 1, 2, …, 31, the initial state of the bits that form the CRC. Bit b_0 is the least significant bit, and Bit b_{31} is the most significant.
- g_i, i = 0, 1, 2, …, 31 are the coefficients of the generating polynomial defined by the IEEE802.3 standard as follows:

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1 \quad (53)$$

$$g_0 = g_1 = g_2 = g_4 = g_5 = g_7 = 1$$
$$g_8 = g_{10} = g_{11} = g_{12} = g_{16} = g_{22} = g_{23} = g_{26} = 1 \quad (54)$$

All of the other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \text{ XOR } b_{31}(j-1) \quad (55)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (56)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, ..., 31 \quad (57)$$

Equation (55), Equation (56), and Equation (57) must be repeated for j = 1, 2, …, 2400. The value written into the CHECKSUM register contains the Bits $b_i(2400)$, i = 0, 1, …, 31.

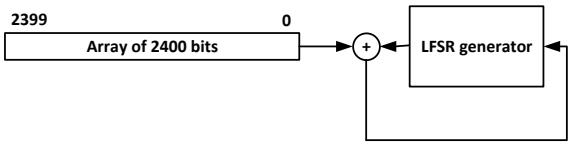


Figure 78. CHECKSUM Register Calculation

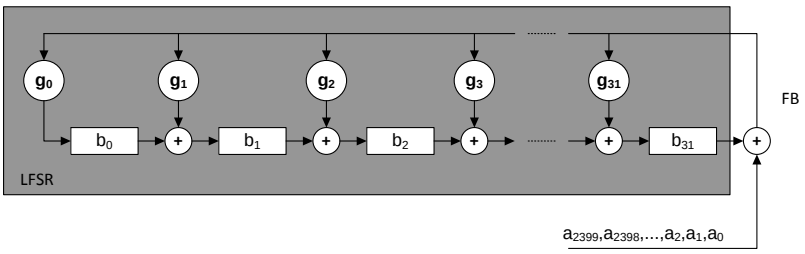


Figure 79. LFSR Generator Used in CHECKSUM Register Calculation

Every time a configuration register of the ADE7978 is written or changes value inadvertently, the Bit 25 (CRC) in STATUS1 register is set to 1 to signal CHECKSUM value has changed. If Bit 25 (CRC) in MASK1 register is set to 1, then the $\overline{\text{IRQ1}}$ interrupt pin is driven low and the status flag CRC in STATUS1 is set to 1. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the status bit set to 1.

When Bit CRC in STATUS1 is set to 1 without any register being written, it can be assumed that one of the registers has changed value and therefore, the ADE7978 has changed configuration. The recommended response is to initiate a hardware/software reset that sets the values of all registers to the default, including the reserved ones, and then reinitialize the configuration registers.

INTERRUPTS

The ADE7978 has two interrupt pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$. Each of the pins is managed by a 32-bit interrupt mask register, MASK0 and MASK1, respectively. To enable an interrupt, a bit in the MASKx register must be set to 1. To disable it, the bit must be cleared to 0. Two 32-bit status registers, STATUS0 and STATUS1, are associated with the interrupts. When an interrupt event occurs in the ADE7978, the corresponding flag in the interrupt status register is set to a logic 1 (see Table 36 and Table 37). If the mask bit for this interrupt in the interrupt mask register is logic 1, then the $\overline{\text{IRQx}}$ logic output goes active low. The flag bits in the interrupt status register are set irrespective of the state of the mask bits. To determine the source of the interrupt, the MCU should perform a read of the corresponding STATUSx register and identify which bit is set to 1. To erase the flag in the status register, write back to the STATUSx register with the flag set to 1. After an interrupt pin goes low, the status register is read and the source of the interrupt is identified. Then, the status register is written back without any change to clear the status flag to 0. The $\overline{\text{IRQx}}$ pin remains low until the status flag is cancelled.

By default, all interrupts are disabled. However, the RSTDONE interrupt is an exception. This interrupt can never be masked (disabled) and, therefore, Bit 15 (RSTDONE) in the MASK1 register does not have any functionality. The $\overline{\text{IRQ1}}$ pin always goes low, and Bit 15 (RSTDONE) in the STATUS1 register is set to 1 whenever a power-up or a hardware/software reset process ends. To cancel the status flag, the STATUS1 register has to be written with Bit 15 (RSTDONE) set to 1.

Certain interrupts are used in conjunction with other status registers. The following bits in the MASK1 register work in conjunction with the status bits in the PHNOLOAD register:

- Bit 0 (NLOAD)
- Bit 1 (FNLOAD)
- Bit 2 (VANLOAD)

The following bits in the MASK1 register work with the status bits in the PHSTATUS register:

- Bit 16, (SAG)
- Bit 17 (OI)
- Bit 18 (OV)

The following bits in the MASK1 register work with the status bits in the IPEAK and VPEAK registers, respectively:

- Bit 23 (PKI)
- Bit 24 (PKV)

The following bits in the MASK0 register work with the status bits in the PHSIGN register:

- Bits[6:8] (REVAPx)
- Bits[10:12] (REVRPx)
- Bit 9, Bit 13, and Bit 18 (REVPSUMx)

When the STATUSx register is read and one of these bits is set to 1, the status register associated with the bit is immediately read to identify the phase that triggered the interrupt and only at that time can the STATUSx register be written back with the bit set to 1.

Using the Interrupts with an MCU

Figure 80 shows a timing diagram that illustrates a suggested implementation of the ADE7978 interrupt management using an MCU. At Time t_1, the $\overline{\text{IRQx}}$ pin goes active low indicating that one or more interrupt events have occurred in the ADE7978, at which point the following steps should be taken:

1. Tie the $\overline{\text{IRQx}}$ pin to a negative-edge-triggered external interrupt on the MCU.
2. On detection of the negative edge, configure the MCU to start executing its interrupt service routine (ISR).
3. On entering the ISR, disable all interrupts using the global interrupt mask bit. At this point, the MCU external interrupt flag can be cleared to capture interrupt events that occur during the current ISR.
4. When the MCU interrupt flag is cleared, a read from STATUSx, the interrupt status register, is carried out. The interrupt status register content is used to determine the

source of the interrupt(s) and, hence, the appropriate action to be taken.

5. The same STATUSx content is written back into the ADE7978 to clear the status flag(s) and reset the $\overline{IRQx}$ line to logic high (t_2).

If a subsequent interrupt event occurs during the ISR (t_3), that event is recorded by the MCU external interrupt flag being set again.

On returning from the ISR, the global interrupt mask bit is cleared (same instruction cycle) and the external interrupt flag uses the MCU to jump to its ISR once again. This ensures that the MCU does not miss any external interrupts.

Figure 81 shows a recommended timing diagram when the status bits in the STATUSx registers work in conjunction with bits in other registers. When the $\overline{IRQx}$ pin goes active low, the STATUSx register is read, and if one of these bits is 1, a second status register is read immediately to identify the phase that triggered the interrupt. The name, PHx, in Figure 81 denotes one of the PHSTATUS, IPEAK, VPEAK, or PHSIGN registers. Then, STATUSx is written back to clear the status flag(s).

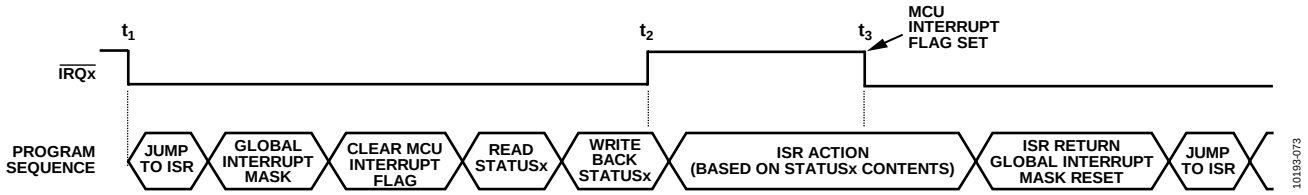


Figure 80. Interrupt Management

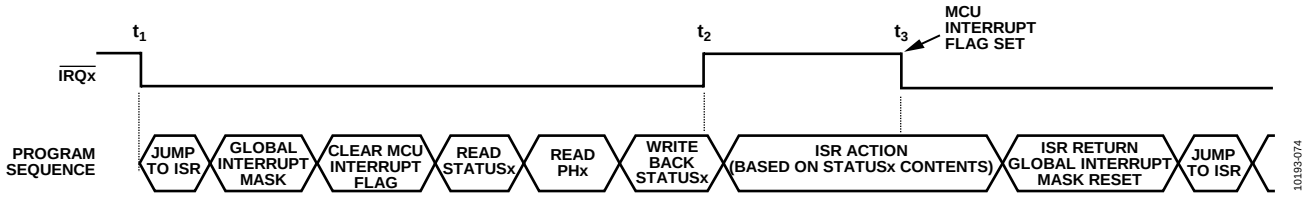


Figure 81. Interrupt Management when PHSTATUS, IPEAK, VPEAK, or PHSIGN Registers are Involved

SERIAL INTERFACES

The ADE7978 has three serial port interfaces: one fully licensed I²C interface, one serial peripheral interface (SPI), and one high speed data capture port (HSDC). As the SPI pins are multiplexed with some of the pins of the I²C and HSDC ports, the ADE7978 accepts two configurations: one using the SPI port only and one using the I²C port in conjunction with the HSDC port.

Serial Interface Choice

After reset, the HSDC port is always disabled. Choose between the I²C and SPI ports by manipulating the $\overline{SS}$/HSA pin after power-up or after a hardware reset. If the $\overline{SS}$/HSA pin is kept high, then the ADE7978 uses the I²C port until a new hardware reset is executed. If the $\overline{SS}$/HSA pin is toggled high to low three times after power-up or after a hardware reset, the ADE7978 uses the SPI port until a new hardware reset is executed. This manipulation of the $\overline{SS}$/HSA pin can be accomplished in two ways. First, use the $\overline{SS}$/HSA pin of the master device (that is, the microcontroller) as a regular I/O pin and toggle it three times. Second, execute three SPI write operations to a location in the address space that is not allocated to a specific ADE7978 register (for example 0xEBFF, where writes to 8-bit registers can be executed). These writes allow the $\overline{SS}$/HSA pin to toggle three times. See the SPI Write Operation section for details on the write protocol involved.

After the serial port choice is completed, it needs to be locked. Consequently, the active port remains in use until a hardware reset or until a power-down. If I²C is the active serial port, Bit 0 (I2C_LOCK) of the CONFIG2 register must be set to 1 to lock it in. From this moment, the ADE7978 ignores spurious toggling of the $\overline{SS}$ pin and an eventual switch into using the SPI port is no longer possible. If the SPI is the active serial port, any write to the CONFIG2 register locks the port. From this moment, a switch into using the I²C port is no longer possible.

The functionality of the ADE7978 is accessible via several on-chip registers. The contents of these registers can be updated or read using either the I²C or SPI interfaces. The HSDC port provides the state of up to 16 registers representing instantaneous values of phase voltages and neutral currents, and active, reactive, and apparent powers.

Communication Verification

The ADE7978 includes a set of three registers that allow any communication via I²C or SPI to be verified. The LAST_OP (Address 0xEA01), LAST_ADD (Address 0xE9FE) and LAST_RWDATA registers record the nature, address and data of the last successful communication respectively. The LAST_RWDATA register has three separate addresses depending on the length of the successful communication.

Table 28. LAST_RWDATA register locations

Communication type	Address
8-Bit Read/Write	0xE7FD
16-Bit Read/Write	0xE9FF
24-Bit Read/Write	0xE5FF

After each successful communication with the ADE7978, the address of the register that was last accessed is stored in the 16-bit LAST_ADD register (Address 0xE9FE). This is a read only register that stores the value until the next successful read or write is complete. Note that when a register located between addresses 0xE50C and 0xE525 is accessed using the SPI communication, the LAST_ADD register stores the address of the register incremented by 1. If the I2C communication is used to address these registers, the LAST_ADD register stores the address of the register. These registers together with the CITHD register located at address 0xE526 can be accessed in burst read operations. See I²C Burst Read Operation and SPI Burst Read Operation sections for details.

The LAST_OP register (Address 0xEA01) stores the nature of the operation. That is, it indicates whether a read or a write was performed. If the last operation is a write, the LAST_OP register stores the value 0xCA. If the last operation is a read, the LAST_OP register stores the value 0x35. The LAST_RWDATA register stores the data that was written or read from the register. Any unsuccessful read or write operation is not reflected in these registers.

When LAST_OP, LAST_ADD and LAST_RWDATA registers are read, their values are not stored into themselves.

I²C-Compatible Interface

The ADE7978 supports a fully licensed I²C interface. The I²C interface is implemented as a full hardware slave. SDA is the data I/O pin, and SCL is the serial clock. These two pins are shared with the MOSI and SCLK pins of the on-chip SPI interface. The maximum serial clock frequency supported by this interface is 400 kHz.

The two pins used for data transfer, SDA and SCL, are configured in a wire-AND'ed format that allows arbitration in a multimaster system.

The transfer sequence of an I²C system consists of a master device initiating a transfer by generating a start condition while the bus is idle. The master transmits the address of the slave device and the direction of the data transfer in the initial address transfer. If the slave acknowledges, the data transfer is initiated. This continues until the master issues a stop condition, and the bus becomes idle.

I²C Write Operation

The write operation using the I²C interface of the ADE7978 initiate when the master generates a start condition and consists in one byte representing the address of the ADE7978 followed by the 16-bit address of the target register and by the value of the register.

The most significant seven bits of the address byte constitute the address of the ADE7978 and they are equal to 0111000b. Bit 0 of the address byte is a read/write bit. Because this is a write operation, it has to be cleared to 0; therefore, the first byte of the write operation is 0x70. After every byte is received, the ADE7978 generates an acknowledge. As registers can have 8, 16, or 32 bits, after the last bit of the register is transmitted and the ADE7978 acknowledges the transfer, the master generates a stop condition. The addresses and the register content are sent with the most significant bit first. See Figure 82 for details of the I²C write operation.

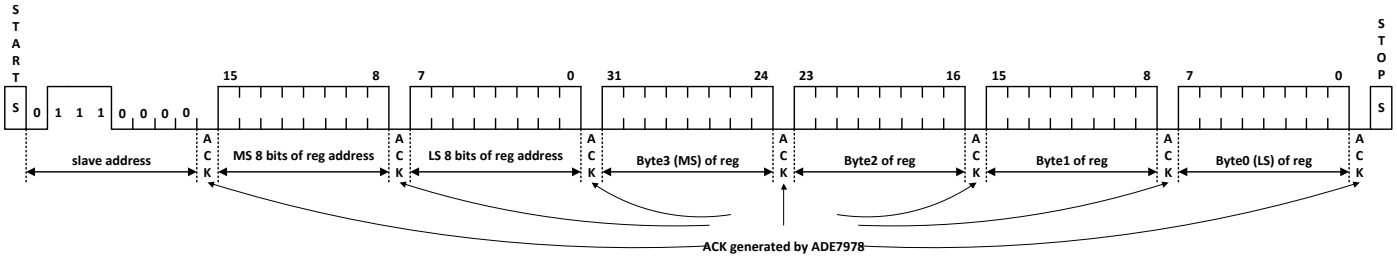


Figure 82. I²C Write Operation of a 32-Bit Register

I²C Read Operation

The read operation using the I²C interface of the ADE7978 is accomplished in two stages. The first stage sets the pointer to the address of the register. The second stage reads the content of the register.

As seen in Figure 83, the first stage initiates when the master generates a start condition and consists in one byte representing the address of the ADE7978 followed by the 16-bit address of the target register. The ADE7978 acknowledges every byte received. The address byte is similar to the address byte of a write operation and is equal to 0x70 (see the I²C Write Operation section for details). After the last byte of the register address has been sent and acknowledged by the ADE7978, the second stage begins with the master generating a new start condition followed by an address byte. The most significant seven bits of this address byte constitute the address of the ADE7978, and they are equal to 0111000b. Bit 0 of the address byte is a read/write bit. Because this is a read operation, it must be set to 1; thus, the first byte of the read operation is 0x71. After this byte is received, the ADE7978 generates an acknowledge. Then, the ADE7978 sends the value of the register, and after every eight bits are received, the master generates an acknowledge. All the bytes are sent with the most significant bit first. Because registers can have 8, 16, or 32 bits, after the last bit of the register is received, the master does not acknowledge the transfer but generates a stop condition.

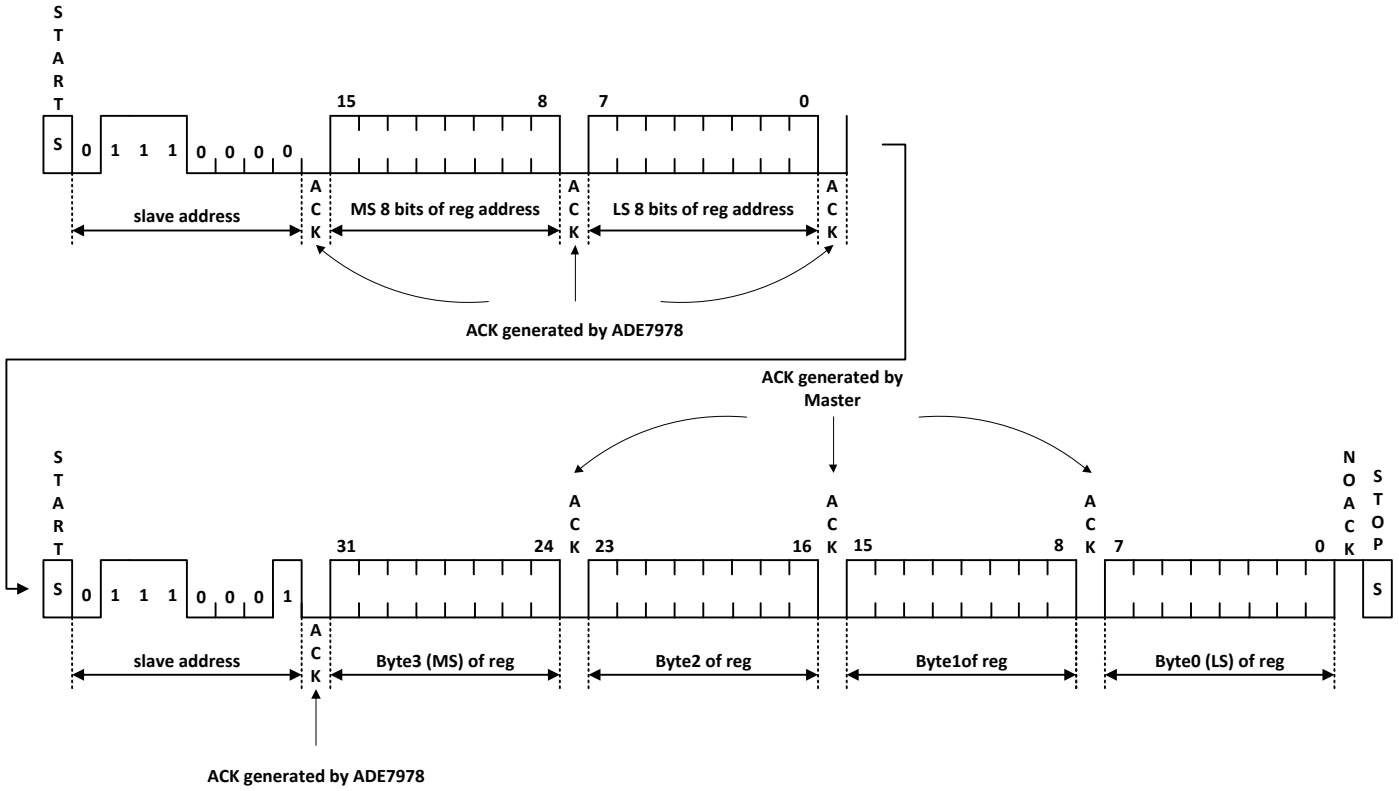


Figure 83. I²C Read Operation of a 32-Bit Register

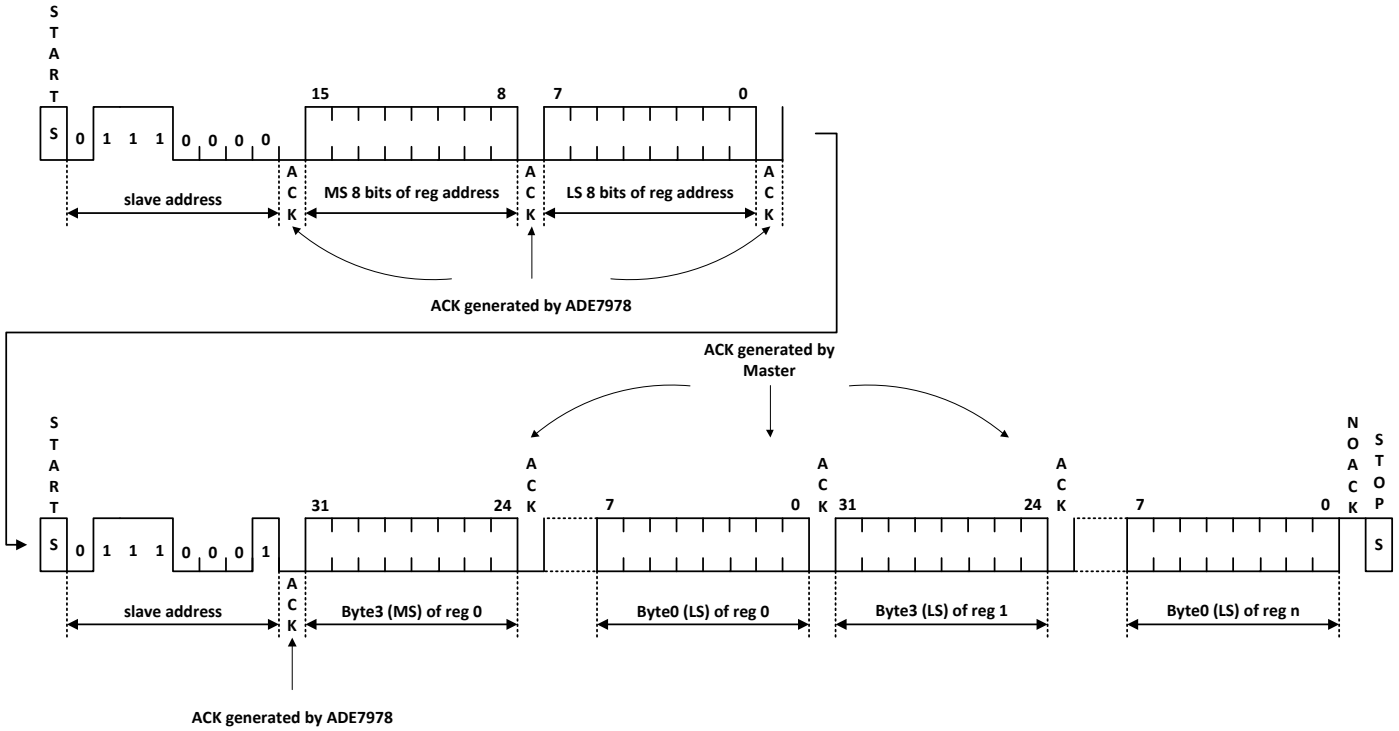


Figure 84. I²C Burst Read Operation of n Consecutive Registers Placed Between 0xE50C and 0xE526 Addresses

I²C Burst Read Operation

The registers between addresses 0xE50C and 0xE526 represent quantities computed by the ADE7978 every 8 kHz: waveform samples (IAWV, IBWV, ICWV, INWV, VAWV, VBWV, VCWV, VA2WV, VB2WV, VC2WV, VNWV, VN2WV), instantaneous values of various powers (AWATT, BWATT, CWATT, AVAR, BVAR, CVAR, AVA, BVA, CVA) and total harmonic distortion (AVTHD, AITHD, BVTHD, BITHD, CVTHD, CITHD). These registers may be read in two ways: one register at a time (see the I²C Read Operation section for details) or multiple consecutive registers at a time in a burst mode. This burst mode is accomplished in two stages. As seen in Figure 84, the first stage sets the pointer to the address of the first register in the burst and is identical to the first stage executed when only one register is read. Any register from the list above may be the first register in the burst. The second stage reads the content of the registers. The second stage begins with the master generating a new start condition followed by an address byte equal to the address byte used when one single register is read, 0x71. After this byte is received, the ADE7978 generates an acknowledge. Then, the ADE7978 sends the value of the first register located at the pointer, and after every eight bits are received, the master generates an acknowledge. All the bytes are sent with the most significant bit first. After the bytes of the first register are sent, if the master acknowledges the last byte, the ADE7978 increments the pointer by one location to position it at the next register and begins to send it out byte by byte, most significant bit first. If the master acknowledges the last byte, the ADE7978 increments the pointer again and begins to send data from the next register. The process continues until the master ceases to generate an acknowledge at the last byte of the register and then generates a stop condition.

It is recommended to not allow burst reading of the locations with addresses greater then 0xE536, the last location of the memory range allocated to this operation.

ZX/$\overline{\text{DREADY}}$ pin, when $\overline{\text{DREADY}}$ functionality is selected (bits 1,0, ZX_DREADY equal to 00 in CONFIG register), goes low 6.5µs before bit 17 (DREADY) in STATUS0 register is set to 1. It stays low for 10µs and then it goes back high. Use its low to high transition to initiate a burst read operation.

SPI-Compatible Interface

The SPI of the ADE7978 is always a slave of the communication and consists of four pins (with dual functions): SCLK/SCL, MOSI/SDA, MISO/HSD, and $\overline{\text{SS}}$/HSA. The functions used in the SPI-compatible interface are SCLK, MOSI, MISO, and $\overline{\text{SS}}$. The serial clock for a data transfer is applied at the SCLK logic input. All data transfer operations synchronize to the serial clock. Data shifts into the ADE7978 at the MOSI logic input on the falling edge of SCLK and the ADE7978 samples it on the rising edge of SCLK. Data shifts out of the ADE7978 at the MISO logic output on a falling edge of SCLK and can be sampled by the master device on the raising edge of SCLK. The most significant bit of the word is shifted in and out first. The maximum serial clock frequency supported by this interface is 2.5 MHz. MISO stays in high impedance when no data is transmitted from the ADE7978. See Figure 85 for details of the connection between the ADE7978 SPI and a master device containing an SPI interface.

The $\overline{\text{SS}}$ logic input is the chip select input. This input is used when multiple devices share the serial bus. Drive the $\overline{\text{SS}}$ input low for the entire data transfer operation. Bringing $\overline{\text{SS}}$ high during a data transfer operation aborts the transfer and places the serial bus in a high impedance state. A new transfer can then be initiated by returning the $\overline{\text{SS}}$ logic input to low. However, because aborting a data transfer before completion leaves the accessed register in a state that cannot be guaranteed, every time a register is written, its value should be verified by reading it back. The protocol is similar to the protocol used in I²C interface.

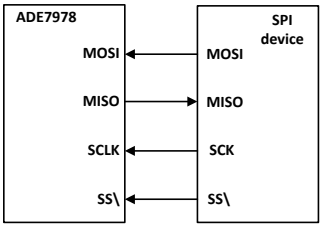


Figure 85. Connecting ADE7978 SPI with an SPI Device

SPI Read Operation

The read operation using the SPI interface of the ADE7978 initiate when the master sets the $\overline{\text{SS}}$/HSA pin low and begins sending one byte, representing the address of the ADE7978, on the MOSI line. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE7978 samples data on the low-to-high transitions of SCLK. The most significant seven bits of the address byte can have any value, but as a good programming practice, they should be different from 0111000b, the seven bits used in the I²C protocol. Bit 0 (read/$\overline{\text{write}}$) of the address byte must be 1 for a read operation. Next, the master sends the 16-bit address of the register that is read. After the ADE7978 receives the last bit of address of the register on a low-to-high transition of SCLK, it begins to transmit its contents on the MISO line when the next SCLK high-to-low transition occurs; thus, the master can sample the data on a low-to-high SCLK transition. After the master receives the last bit, it sets the $\overline{\text{SS}}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 86 for details of the SPI read operation.

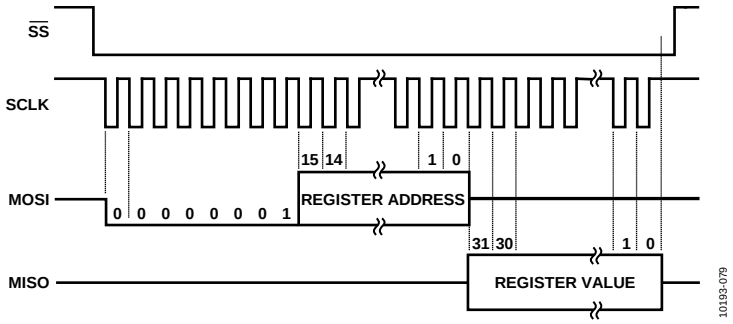


Figure 86. SPI Read Operation of a 32-Bit Register

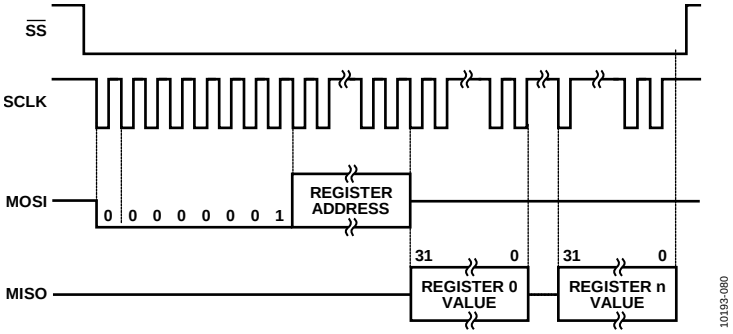


Figure 87. SPI Read Operation of n Consecutive Registers Placed between 0xE50C and 0xE526 addresses

SPI Burst Read Operation

The registers between addresses 0xE50C and 0xE526 (see I²C Burst Read Operation for the list of the registers) may be read in two ways: one register at a time (see the SPI Read Operation section for details) or multiple consecutive registers at a time in a burst mode. The burst mode initiates when the master sets the $\overline{SS}$/HSA pin low and begins sending one byte, representing the address of the ADE7978, on the MOSI line. The address is the same address byte used for reading only one register. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE7978 samples data on the low-to-high transitions of SCLK. Next, the master sends the 16-bit address of the first register in the burst that is read. Any register located between addresses 0xE50C and 0xE526 may be the first register in the burst. After the ADE7978 receives the last bit of the address of the register on a low-to-high transition of SCLK, it begins to transmit its contents on the MISO line when the next SCLK high-to-low transition occurs; thus, the master can sample the data on a low-to-high SCLK transition. After the master receives the last bit of the first register, the ADE7978 sends the harmonic calculations register placed at the next location and so forth until the master sets the $\overline{SS}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 87 for details of the SPI burst read operation.

It is recommended to not allow burst reading of the locations with addresses greater then 0xE536, the last location of the memory range allocated to this operation.

ZX/$\overline{DREADY}$ pin, when $\overline{DREADY}$ functionality is selected (bits 1,0, ZX_DREADY equal to 00 in CONFIG register), goes low 6.5µs before bit 17 (DREADY) in STATUS0 register is set to 1. It stays low for 10µs and then goes back high. Us its low to high transition to initiate a burst read operation.

SPI Write Operation

The write operation using the SPI interface of the ADE7978 initiates when the master sets the $\overline{SS}$/HSA pin low and begins sending one byte representing the address of the ADE7978 on the MOSI line. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE7978 samples data on the low-to-high transitions of SCLK. The most significant seven bits of the address byte can have any value, but as a good programming practice, they should be different from 0111000b, the seven bits used in the I²C protocol. Bit 0 (read/$\overline{write}$) of the address byte must be 0 for a write operation. Next, the master sends the 16-bit address of the register that is written and the 32-, 16-, or 8-bit value of that register without losing any SCLK cycle. After the last bit is transmitted, the master sets the $\overline{SS}$ and SCLK lines high at the end of the SCLK cycle and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 88 for details of the SPI write operation.

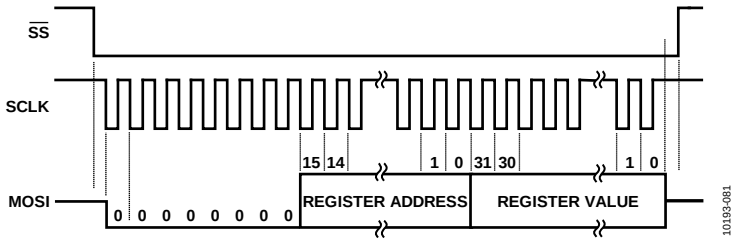


Figure 88. SPI Write Operation of a 32-Bit Register

HSDC Interface

The high speed data capture (HSDC) interface is disabled after default. It can be used only if the ADE7978 is configured with an I^2C interface. The SPI interface of the ADE7978 cannot be used at the same time with HSDC.

Bit 6 (HSDCEN) in the CONFIG register activates HSDC when set to 1. If Bit HSDCEN is cleared to 0, the default value, the HSDC interface is disabled. Setting Bit HSDCEN to 1 when SPI is in use does not have any effect. HSDC is an interface for sending to an external device (usually a microprocessor or a DSP) up to sixteen 32-bit words. The words represent the instantaneous values of the phase currents and voltages, neutral current, and active, reactive, and apparent powers. The registers being transmitted include IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, INWV, AVA, BVA, CVA, AWATT, BWATT, CWATT, AVAR, BVAR, and CVAR. All are 24-bit registers that are sign extended to 32-bits (see Figure 34 for details).

HSDC can be interfaced with SPI or similar interfaces. HSDC is always a master of the communication and consists of three pins: HSA, HSD, and HSCLK. HSA represents the select signal. It stays active low or high when a word is transmitted and it is usually connected to the select pin of the slave. HSD sends data to the slave and it is usually connected to the data input pin of the slave. HSCLK is the serial clock line that is generated by the ADE7978 and it is usually connected to the serial clock input of the slave. Figure 89 shows the connections between the ADE7978 HSDC and slave devices containing an SPI interface.

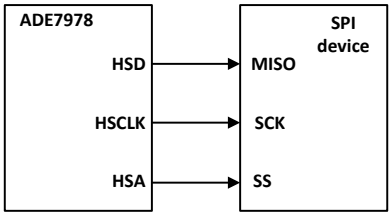


Figure 89. Connecting the ADE7978 HSDC with an SPI

The HSDC communication is managed by the HSDC_CFG register (see Table 51). It is recommended to set the HSDC_CFG register to the desired value before enabling the port using Bit 6 (HSDCEN) in the CONFIG register. In this way, the state of various pins belonging to the HSDC port do not take levels inconsistent with the desired HSDC behavior. After a hardware reset or after power-up, the MISO/HSD and $\overline{SS}$/HSA pins are set high.

Bit 0 (HCLK) in the HSDC_CFG register determines the serial clock frequency of the HSDC communication. When HCLK is 0 (the default value), the clock frequency is 8 MHz. When HCLK is 1, the clock frequency is 4 MHz. A bit of data is transmitted for every HSCLK high-to-low transition. The slave device that receives data from HSDC samples the HSD line on the low-to-high transition of HSCLK.

The words can be transmitted as 32-bit packages or as 8-bit packages. When Bit 1 (HSIZE) in the HSDC_CFG register is 0 (the default value), the words are transmitted as 32-bit packages. When Bit HSIZE is 1, the registers are transmitted as 8-bit packages. The HSDC interface transmits the words MSB first.

Bit 2 (HGAP) introduces a gap of seven HSCLK cycles between packages when Bit 2 (HGAP) is set to 1. When Bit HGAP is cleared to 0 (the default value), no gap is introduced between packages and the communication time is shortest. In this case, HSIZE does not have any influence on the communication and a data bit is placed on the HSD line with every HSCLK high-to-low transition.

Bits[4:3] (HXFER[1:0]) decide how many words are transmitted. When HXFER[1:0] is 00, the default value, then all 16 words are transmitted. When HXFER[1:0] is 01, only the words representing the instantaneous values of phase and neutral currents and phase voltages are transmitted in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, and INWV. When HXFER[1:0] is 10, only the instantaneous values of phase powers are transmitted in the following order: AVA, BVA, CVA, AWATT, BWATT, CWATT, AVAR, BVAR, and CVAR. The value, 11, for HXFER[1:0] is reserved and writing it is equivalent to writing 00, the default value.

Bit 5 (HSAPOL) determines the polarity of HSA function of the $\overline{SS}$/HSA pin during communication. When HSAPOL is 0 (the default value), HSA is active low during the communication. This means that HSA stays high when no communication is in progress. When a communication is executed, HSA is low when the 32-bit or 8-bit packages are transferred and is high during the gaps. When HSAPOL is 1, the HSA function of the $\overline{SS}$/HSA pin is active high during the communication. This means that HSA stays low when no communication is in progress. When a communication is executed, HSA is high when the 32-bit or 8-bit packages are transferred and is low during the gaps.

Bits[7:6] of the HSDC_CFG register are reserved. Any value written into these bits does not have any consequence on HSDC behavior.

Figure 90 shows the HSDC transfer protocol for HGAP = 0, HXFER[1:0] = 00 and HSAPOL = 0. Note that the HSDC interface sets a data bit on the HSD line every HSCLK high-to-low transition and the value of Bit HSIZE is irrelevant.

Figure 91 shows the HSDC transfer protocol for HSIZE = 0, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0. Note that the HSDC interface introduces a seven-HSCLK cycles gap between every 32-bit word.

Figure 92 shows the HSDC transfer protocol for HSIZE = 1, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0. Note that the HSDC interface introduces a seven-HSCLK cycles gap between every 8-bit word.

See Table 51 for the HSDC_CFG register and descriptions for the HCLK, HSIZE, HGAP, HXFER[1:0], and HSAPOL bits. Table 29 lists the time it takes to execute an HSDC data transfer for all HSDC_CFG register settings. For some settings, the transfer time is less than 125 µs (8 kHz), the waveform sample registers update rate. This means the HSDC port transmits data every sampling cycle. For settings in which the transfer time is greater than 125 µs, the HSDC port transmits data only in the first of two consecutive 8 kHz sampling cycles. This means it transmits registers at an effective rate of 4 kHz.

Table 29. Communication Times for Various HSDC Settings

HXFER[1:0]	HGAP	HSIZE[1]	HCLK	Communication Time (µs)
00	0	N/A	0	64
00	0	N/A	1	128
00	1	0	0	77.125
00	1	0	1	154.25
00	1	1	0	119.25
00	1	1	1	238.25
01	0	N/A	0	28
01	0	N/A	1	56
01	1	0	0	33.25
01	1	0	1	66.5
01	1	1	0	51.625
01	1	1	1	103.25
10	0	N/A	0	36
10	0	N/A	1	72
10	1	0	0	43
10	1	0	1	86
10	1	1	0	66.625
10	1	1	1	133.25

[1] N/A means not applicable.

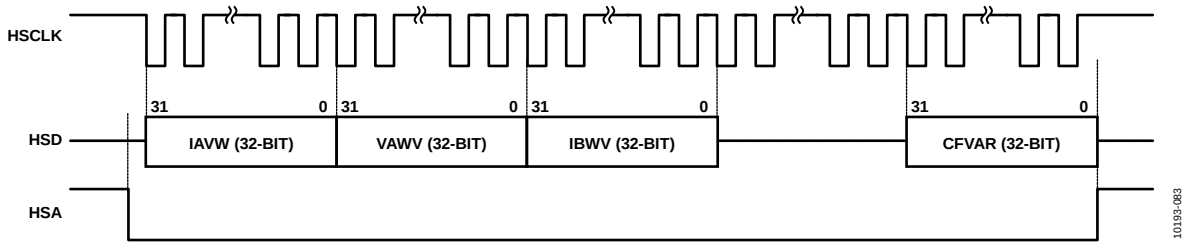


Figure 90. HSDC Communication for HGAP = 0, HXFER[1:0] = 00, and HSAPOL = 0; HSIZE Is Irrelevant

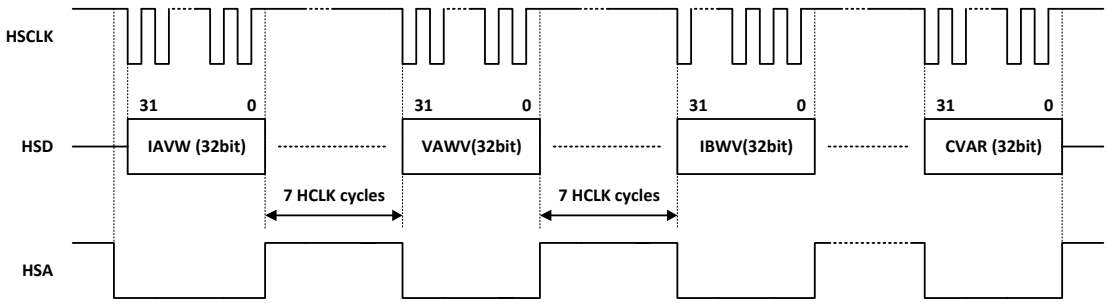


Figure 91. HSDC Communication for HSIZE = 0, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0

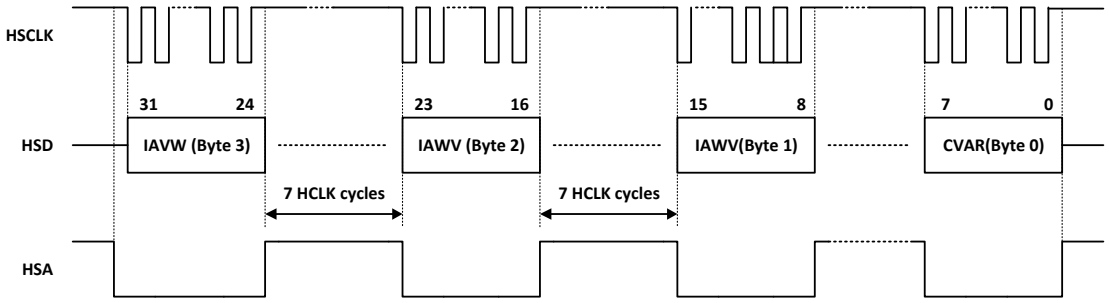


Figure 92. HSDC Communication for HSIZE = 1, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADE7933/ADE7932 devices. Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 16 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases. The insulation lifetime of the ADE7933/ADE7932 devices depends on the voltage waveform type imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 93, Figure 94, and Figure 95 illustrate these different isolation voltage waveforms. Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the bipolar ac condition determines the maximum working voltage recommended by Analog Devices. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 16 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 94 or Figure 95 should be treated as a bipolar ac waveform and its peak voltage limited to the 50-year lifetime voltage value listed in Table 16. The voltage presented in Figure 94 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

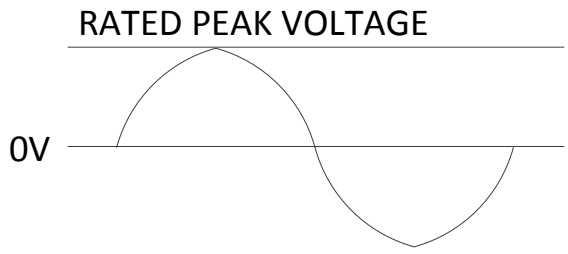


Figure 93. BipolarAC Waveform

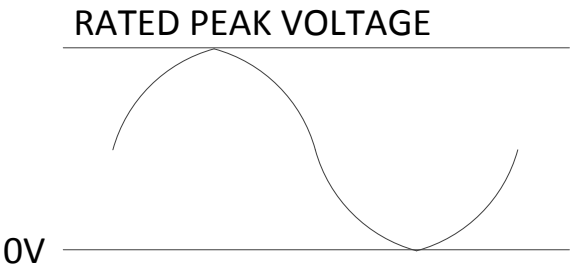


Figure 94.Unipolar AC Waveform

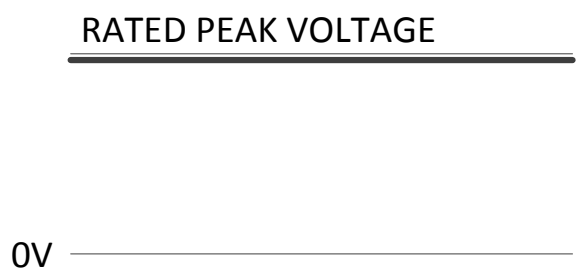


Figure 95. DC Waveform

ADE7978 QUICK SETUP AS ENERGY METER

An energy meter is usually characterized by the nominal current I_n, nominal voltage V_n, nominal frequency f_n, and the meter constant MC.

To quickly set up the ADE7978, execute the following steps:

1. If f_n = 60 Hz, set Bit 14 (SELFREQ) to 1 in the COMPMODE register.
2. Initialize CF1DEN, CF2DEN, and CF3DEN registers based in Equation (50).
3. Initialize WTHR, VARTHR, VATHR, VLEVEL and VNOM registers based Equation (31), Equation (38), Equation (45), Equation(28), and Equation(43), respectively.
4. Enable the data memory RAM protection, by writing 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.
5. Start the DSP by setting Run = 1.

ADE7978 AND ADE7933/ADE7932 EVALUATION BOARD

An evaluation board built upon the ADE7978 and ADE7933/ADE7932 chipset configuration is available. Visit TBD website for details.

ADE7978 DIE VERSION

The register named version identifies the version of the ADE7978 die. It is an 8-bit, read-only register located at Address 0xE707.

REGISTERS LIST

Table 30. Registers List Located in DSP Data Memory RAM

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x4380	AIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A current gain adjust.
0x4381	AVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A voltage gain adjust.
0x4382	AV2GAIN	R/W	24	32 ZPSE	S	0x000000	Phase A V2P channel gain adjust.
0x4383	BIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B current gain adjust.
0x4384	BVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B voltage gain adjust.
0x4385	BV2GAIN	R/W	24	32 ZPSE	S	0x000000	Phase B V2P channel gain adjust.
0x4386	CIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C current gain adjust.
0x4387	CVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C voltage gain adjust.
0x4388	CV2GAIN	R/W	24	32 ZPSE	S	0x000000	Phase C V2P channel gain adjust.
0x4389	NIGAIN	R/W	24	32 ZPSE	S	0x000000	Neutral current rms offset.
0x438A	NVGAIN	R/W	24	32 ZPSE	S	0x000000	Neutral line V1P channel gain adjust.
0x438B	NV2GAIN	R/W	24	32 ZPSE	S	0x000000	Neutral line V2P channel gain adjust.
0x438C	AIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A current rms offset.
0x438D	AVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A voltage rms offset.
0x438E	AV2RMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A V2P voltage rms offset.
0x438F	BIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B current rms offset.
0x4390	BVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B voltage rms offset.
0x4391	BV2RMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B V2P voltage rms offset.
0x4392	CIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C current rms offset.
0x4393	CVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C voltage rms offset.
0x4394	CV2RMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C V2P voltage rms offset.
0x4395	NIRMSOS	R/W	24	32 ZPSE	S	0x000000	Neutral current rms offset.
0x4396	NVRMSOS	R/W	24	32 ZPSE	S	0x000000	Neutral line V1P voltage rms offset.
0x4397	NV2RMSOS	R/W	24	32 ZPSE	S	0x000000	Neutral line V2P voltage rms offset.
0x4398	ISUMLVL	R/W	24	32 ZPSE	S	0x000000	Threshold used in comparison between the sum of phase currents and the neutral current.
0x4399	APGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A power gain adjust.
0x439A	BPGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B power gain adjust.
0x439B	CPGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C power gain adjust.
0x439C	AWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase A total active power offset adjust.
0x439D	BWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase B total active power offset adjust.
0x439E	CWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase C total active power offset adjust.
0x439F	AVAROS	R/W	24	32 ZPSE	S	0x000000	Phase A total reactive power offset adjust.
0x43A0	BVAROS	R/W	24	32 ZPSE	S	0x000000	Phase B total reactive power offset adjust.
0x43A1	CVAROS	R/W	24	32 ZPSE	S	0x000000	Phase C total reactive power offset adjust.
0x43A2	VLEVEL	R/W	24	32 ZPSE	S	0x000000	Register used in the algorithm that computes the fundamental active and reactive powers. See expression (28).
0x43A3	AFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental active power offset adjust.
0x43A4	BFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental active power offset adjust.
0x43A5	CFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental active power offset adjust.
0x43A6	AFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental reactive power offset adjust.
0x43A7	BFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental reactive power offset adjust.
0x43A8	CFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental reactive power offset adjust.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x43A9	AFIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental current rms offset.
0x43AA	BFIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental current rms offset.
0x43AB	CFIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental current rms offset.
0x43AC	AFVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental voltage rms offset.
0x43AD	BFVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental voltage rms offset.
0x43AE	CFVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental voltage rms offset.
0x43AF	TEMPCO	R/W	24	32 ZPSE	S	0x000000	Shunts temperature coefficent.
0x43B0	ATEMP0	R/W	24	32 ZPSE	S	0x000000	Phase A ADE7933/ADE7932 ambient temperature at calibration.
0x43B1	BTEMP0	R/W	24	32 ZPSE	S	0x000000	Phase B ADE7933/ADE7932 ambient temperature at calibration.
0x43B2	CTEMP0	R/W	24	32 ZPSE	S	0x000000	Phase C ADE7933/ADE7932 ambient temperature at calibration.
0x43B3	NTEMP0	R/W	24	32 ZPSE	S	0x000000	Neutral line ADE7933/ADE7932 ambient temperature at calibration.
0x43B4	ATGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A temperature gain adjust.
0x43B5	BTGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B temperature gain adjust.
0x43B6	CTGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C temperature gain adjust.
0x43B7	NTGAIN	R/W	24	32 ZPSE	S	0x000000	Neutral line temperature gain adjust.
0x43B8 to 0x43BF	Reserved	N/A[4]	N/A	N/A	N/A	0x000000	These memory locations should be kept at 0x000000 for proper operation.
0x43C0	AIRMS	R	24	32 ZP	S	N/A	Phase A current rms value.
0x43C1	AVRMS	R	24	32 ZP	S	N/A	Phase A voltage rms value.
0x43C2	AV2RMS	R	24	32 ZP	S	N/A	Phase A V2P voltage rms value.
0x43C3	BIRMS	R	24	32 ZP	S	N/A	Phase B current rms value.
0x43C4	BVRMS	R	24	32 ZP	S	N/A	Phase B voltage rms value.
0x43C5	BV2RMS	R	24	32 ZP	S	N/A	Phase B V2P voltage rms value.
0x43C6	CIRMS	R	24	32 ZP	S	N/A	Phase C current rms value.
0x43C7	CVRMS	R	24	32 ZP	S	N/A	Phase C voltage rms value.
0x43C8	CV2RMS	R	24	32 ZP	S	N/A	Phase C V2P voltage rms value.
0x43C9	NIRMS	R	24	32 ZP	S	N/A	Neutral current rms value.
0x43CA	ISUM	R	28	32 ZP	S	N/A	Sum of IAWV, IBWV, and ICWV registers.
0x43CB	ATEMP	R	24	32 ZP	S	N/A	Phase A ADE7933/ADE7932 temperature.
0x43CC	BTEMP	R	24	32 ZP	S	N/A	Phase B ADE7933/ADE7932 temperature.
0x43CD	CTEMP	R	24	32 ZP	S	N/A	Phase C ADE7933/ADE7932 temperature.
0x43CE	NTEMP	R	24	32 ZP	S	N/A	Neutral line ADE7933/ADE7932 temperature.
0x43CF to 0x43FF	Reserved	N/A	N/A	N/A	N/A	0x000000	These memory locations should be kept at 0x000000 for proper operation.

[1] R is read, and W is write.
[2] 32 ZPSE = 24-bit signed register that is transmitted as a 32-bit word with four MSBs padded with 0s and sign extended to 28 bits. Whereas 32 ZP = 28- or 24-bit signed or unsigned register that is transmitted as a 32-bit word with four MSBs or eight MSBs, respectively, padded with 0s.
[3] U is unsigned register, and S is signed register in twos complement format.
[4] N/A means not applicable.

Table 31. Internal DSP Memory RAM Registers

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication	Type[2]	Default Value	Description
0xE203	Reserved	R/W	16	16	U	0x0000	This memory location should not be written for proper operation.
0xE228	Run	R/W	16	16	U	0x0000	Run register starts and stops the DSP. See the Digital Signal Processor section for more details.

[1] R is read, and W is write.
[2] U is unsigned register, and S is signed register in twos complement format.

Table 32. Billable Registers

Address	Register Name	R/W[1, 2]	Bit Length[2]	Bit Length During Communication[2]	Type[2, 3]	Default Value	Description
0xE400	AWATTHR	R	32	32	S	0x00000000	Phase A total active energy accumulation.
0xE401	BWATTHR	R	32	32	S	0x00000000	Phase B total active energy accumulation.
0xE402	CWATTHR	R	32	32	S	0x00000000	Phase C total active energy accumulation.
0xE403	AFWATTHR	R	32	32	S	0x00000000	Phase A fundamental active energy accumulation.
0xE404	BFWATTHR	R	32	32	S	0x00000000	Phase B fundamental active energy accumulation.
0xE405	CFWATTHR	R	32	32	S	0x00000000	Phase C fundamental active energy accumulation.
0xE406	AVARHR	R	32	32	S	0x00000000	Phase A total reactive energy accumulation.
0xE407	BVARHR	R	32	32	S	0x00000000	Phase B total reactive energy accumulation.
0xE408	CVARHR	R	32	32	S	0x00000000	Phase C total reactive energy accumulation.
0xE409	AFVARHR	R	32	32	S	0x00000000	Phase A fundamental reactive energy.
0xE40A	BFVARHR	R	32	32	S	0x00000000	Phase B fundamental reactive energy.
0xE40B	CFVARHR	R	32	32	S	0x00000000	Phase C fundamental reactive energy.
0xE40C	AVAHR	R	32	32	S	0x00000000	Phase A apparent energy accumulation.
0xE40D	BVAHR	R	32	32	S	0x00000000	Phase B apparent energy accumulation.
0xE40E	CVAHR	R	32	32	S	0x00000000	Phase C apparent energy accumulation.

[1] R is read, and W is write.
[2] N/A is not applicable.
[3] U is unsigned register, and S is signed register in twos complement format.

Table 33. Configuration and Power Quality Registers

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE500	IPEAK	R	32	32	U	N/A	Current peak register. See Figure 48 and Table 34 for details about its composition.
0xE501	VPEAK	R	32	32	U	N/A	Voltage peak register. See Figure 48 and Table 35 for details about its composition.
0xE502	STATUS0	R/W	32	32	U	N/A	Interrupt Status Register 0. See Table 36.
0xE503	STATUS1	R/W	32	32	U	N/A	Interrupt Status Register 1. See Table 37.
0xE504 to 0xE506	Reserved						These addresses should not be written for proper operation.
0xE507	OILVL	R/W	24	32 ZP	U	0xFFFFFF	Overcurrent threshold.
0xE508	OVLVL	R/W	24	32 ZP	U	0xFFFFFF	Overvoltage threshold.
0xE509	SAGLVL	R/W	24	32 ZP	U	0x000000	Voltage SAG level threshold.
0xE50A	MASK0	R/W	32	32	U	0x00000000	Interrupt Enable Register 0. See Table 38.

Address	Register Name	R/W [1]	Bit Length	Bit Length During Communication [2]	Type [3]	Default Value [4]	Description
0xE50B	MASK1	R/W	32	32	U	0x00000000	Interrupt Enable Register 1. See Table 39.
0xE50C	IAWV	R	24	32 SE	S	N/A	Instantaneous value of Phase A current.
0xE50D	IBWV	R	24	32 SE	S	N/A	Instantaneous value of Phase B current.
0xE50E	ICWV	R	24	32 SE	S	N/A	Instantaneous value of Phase C current.
0xE50F	INWV	R	24	32 SE	S	N/A	Instantaneous value of neutral current.
0xE510	VAWV	R	24	32 SE	S	N/A	Instantaneous value of Phase A voltage.
0xE511	VBWV	R	24	32 SE	S	N/A	Instantaneous value of Phase B voltage.
0xE512	VCWV	R	24	32 SE	S	N/A	Instantaneous value of Phase C voltage.
0xE513	VA2WV	R	24	32 SE	S	N/A	Instantaneous value of Phase A V2P voltage.
0xE514	VB2WV	R	24	32 SE	S	N/A	Instantaneous value of Phase B V2P voltage.
0xE515	VC2WV	R	24	32 SE	S	N/A	Instantaneous value of Phase C V2P voltage.
0xE516	VNWV	R	24	32 SE	S	N/A	Instantaneous value of Neutral Line V1P voltage.
0xE517	VN2WV	R	24	32 SE	S	N/A	Instantaneous value of Neutral Line V2P voltage.
0xE518	AWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase A total active power.
0xE519	BWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase B total active power.
0xE51A	CWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase C total active power.
0xE51B	AVAR	R	24	32 SE	S	N/A	Instantaneous value of Phase A total reactive power.
0xE51C	BVAR	R	24	32 SE	S	N/A	Instantaneous value of Phase B total reactive power.
0xE51D	CVAR	R	24	32 SE	S	N/A	Instantaneous value of Phase C total reactive power.
0xE51E	AVA	R	24	32 SE	S	N/A	Instantaneous value of Phase A apparent power.
0xE51F	BVA	R	24	32 SE	S	N/A	Instantaneous value of Phase B apparent power.
0xE520	CVA	R	24	32 SE	S	N/A	Instantaneous value of Phase C apparent power.
0xE521	AVTHD	R	24	32 ZP	U	N/A	Total harmonic distortion of Phase A voltage.
0xE522	AITHD	R	24	32 ZP	U	N/A	Total harmonic distortion of Phase A current.
0xE523	BVTHD	R	24	32 ZP	U	N/A	Total harmonic distortion of Phase B voltage.
0xE524	BITHD	R	24	32 ZP	U	N/A	Total harmonic distortion of Phase B current.
0xE525	CVTHD	R	24	32 ZP	U	N/A	Total harmonic distortion of Phase C voltage.
0xE526	CITHD	R	24	32 ZP	U	N/A	Total harmonic distortion of Phase C current.
0xE527 to 0xE52F	Reserved						These addresses should not be written for proper operation.
0xE530	NVRMS	R	24	32 ZP	S	N/A	Neutral Line V1P voltage rms value.
0xE531	NV2RMS	R	24	32 ZP	S	N/A	Neutral Line V2P voltage rms value.
0xE532	CHECKSUM	R	32	32	U	0x6BF87803	Checksum verification. See the Checksum Register section for details.
0xE533	VNOM	R/W	24	32 ZP	S	0x000000	Nominal phase voltage rms used in the

Address	Register Name	R/W [1]	Bit Length	Bit Length During Communication [2]	Type [3]	Default Value [4]	Description
							alternative computation of the apparent power.
0xE534 to 0xE536	Reserved						These addresses should not be written for proper operation.
0xE537	AFIRMS	R	24	32 ZP	S	N/A	Phase A fundamental current rms value.
0xE538	AFVRMS	R	24	32 ZP	S	N/A	Phase A fundamental voltage rms value.
0xE539	BFIRMS	R	24	32 ZP	S	N/A	Phase B fundamental current rms value.
0xE53A	BFVRMS	R	24	32 ZP	S	N/A	Phase B fundamental voltage rms value.
0xE53B	CFIRMS	R	24	32 ZP	S	N/A	Phase C fundamental current rms value.
0xE53C	CFVRMS	R	24	32 ZP	S	N/A	Phase C fundamental voltage rms value.
0xE53D to 0xE5FE	Reserved						These addresses should not be written for proper operation.
0xE5FF	LAST_RWDATA32	R	32	32	U	N/A	Contains the data from the last successful 32-bit register communication.
0xE600	PHSTATUS	R	16	16	U	N/A	Phase peak register. See Table 40.
0xE601	ANGLE0	R	16	16	U	N/A	Time Delay 0. See the Time Interval Between Phases section for details.
0xE602	ANGLE1	R	16	16	U	N/A	Time Delay 1. See the Time Interval Between Phases section for details.
0xE603	ANGLE2	R	16	16	U	N/A	Time Delay 2. See the Time Interval Between Phases section for details.
0xE604 to 0xE607	Reserved						These addresses should not be written for proper operation.
0xE608	PHNOLOAD	R	16	16	U	N/A	Phase no load register. See Table 41.
0xE609 to 0xE60B	Reserved						These addresses should not be written for proper operation.
0xE60C	LINECYC	R/W	16	16	U	0xFFFF	Line cycle accumulation mode count.
0xE60D	ZXTOUT	R/W	16	16	U	0xFFFF	Zero-crossing timeout count.
0xE60E	COMPMODE	R/W	16	16	U	0x01FF	Computation-mode register. See Table 42.
0xE60F	Reserved						This address should not be written for proper operation.
0xE610	CFMODE	R/W	16	16	U	0x0E88	CFx configuration register. See Table 43.
0xE611	CF1DEN	R/W	16	16	U	0x0000	CF1 denominator.
0xE612	CF2DEN	R/W	16	16	U	0x0000	CF2 denominator.
0xE613	CF3DEN	R/W	16	16	U	0x0000	CF3 denominator.
0xE614	APHCAL	R/W	10	16 ZP	U	0x0000	Phase calibration of Phase A. See Table 44.
0xE615	BPHCAL	R/W	10	16 ZP	U	0x0000	Phase calibration of Phase B. See Table 44.
0xE616	CPHCAL	R/W	10	16 ZP	U	0x0000	Phase calibration of Phase C. See Table 44.
0xE617	PHSIGN	R	16	16	U	N/A	Power sign register. See Table 45.
0xE618	CONFIG	R/W	16	16	U	0x0010	ADE7978 configuration register. See Table 46.
0xE700	MMODE	R/W	8	8	U	0x1C	Measurement mode register. See Table 47.
0xE701	ACCMODE	R/W	8	8	U	0x00	Accumulation mode register. See Table 48.
0xE702	LCYCMODE	R/W	8	8	U	0x78	Line accumulation mode behavior. See Table 50.
0xE703	PEAKCYC	R/W	8	8	U	0x00	Peak detection half line cycles.

Address	Register Name	R/W [1]	Bit Length	Bit Length During Communication [2]	Type [3]	Default Value [4]	Description
0xE704	SAGCYC	R/W	8	8	U	0x00	SAG detection half line cycles.
0xE705	CFCYC	R/W	8	8	U	0x01	Number of CF pulses between two consecutive energy latches. See the Synchronizing Energy Registers with CFx Outputs section.
0xE706	HSDC_CFG	R/W	8	8	U	0x00	HSDC configuration register. See Table 51.
0xE707	Version	R	8	8	U		Version of die.
0xE708	CONFIG3	R/W	8	8	U	0x0F	ADE7933/ADE7932s configuration register. See Table 52.
0xE709	ATEMPOS	R	8	8	S	0x00	Phase A ADE7933/ADE7932 temperature sensor offset.
0xE70A	BTEMPOS	R	8	8	S	0x00	Phase B ADE7933/ADE7932 temperature sensor offset.
0xE70B	CTEMPOS	R	8	8	S	0x00	Phase C ADE7933/ADE7932 temperature sensor offset.
0xE70C	NTEMPOS	R	8	8	S	0x00	Neutral line ADE7933/ADE7932 temperature sensor offset.
0xE7FD	LAST_RWDATA8	R	8	8	U	N/A	Contains the data from the last successful 8-bit register communication.
0xE7FE to 0xE901	Reserved						These addresses should not be written for proper operation.
0xE902	APF	R	16	16	U	N/A	Phase A power factor.
0xE903	BPF	R	16	16	U	N/A	Phase B power factor.
0xE904	CPF	R	16	16	U	N/A	Phase C power factor.
0xE905	APERIOD	R	16	16	U	N/A	Line period on Phase A voltage.
0xE906	BPERIOD	R	16	16	U	N/A	Line period on Phase B voltage.
0xE907	CPERIOD	R	16	16	U	N/A	Line period on Phase C voltage.
0xE908	APNOLOAD	R/W	16	16	U	0x0000	No load threshold in the total/ fundamental active power data paths.
0xE909	VARNOLOAD	R/W	16	16	U	0x0000	No load threshold in the total/ fundamental reactive power data path.
0xE90A	VANOLOAD	R/W	16	16	U	0x0000	No load threshold in the apparent power data path.
0xE90B to 0xE9FD	Reserved						These addresses should not be written for proper operation.
0xE9FE	LAST_ADD	R	16	16	U	N/A	The address of the register successfully accessed during the last read/write operation.
0xE9FF	LAST_RWDATA16	R	16	16	U	N/A	Contains the data from the last successful 16-bit register communication.
0xEA00	CONFIG2	R/W	8	8	U		Configuration register. See Table 53 for details.
0xEA01	LAST_OP	R	8	8	U	N/A	Indicates the type, read or write, of the last successful read/write operation.
0xEA02	WTHR	R/W	8	8	U	0x03	Threshold used in phase total/ fundamental active power data path.
0xEA03	VARTHR	R/W	8	8	U	0x03	Threshold used in phase total/ fundamental reactive power data path.
0xEA04	VATHR	R/W	8	8	U	0x03	Threshold used in phase apparent power data path.

Address	Register Name	R/W [1]	Bit Length	Bit Length During Communication [2]	Type [3]	Default Value [4]	Description
0xEA05 to 0xEBFE	Reserved		8	8			This address should not be written for proper operation.
0xEBFF	Reserved		8	8			This address can be used in manipulating the $\overline{SS}$/HSA pin when SPI is chosen as the active port. See the Serial Interfaces section for details.

[1] R is read, and W is write.
[2] 32 ZP = 24- or 20-bit signed or unsigned register that is transmitted as a 32-bit word with 8 or 12 MSBs, respectively, padded with 0s. 32 SE = 24-bit signed register that is transmitted as a 32-bit word sign extended to 32 bits. 16 ZP = 10-bit unsigned register that is transmitted as a 16-bit word with six MSBs padded with 0s.
[3] U is unsigned register, and S is signed register in twos complement format.
[4] N/A is not applicable.

Table 34. IPEAK Register (Address 0xE500)

Bit Location	Bit Mnemonic	Default Value	Description
23:0	IPEAKVAL[23:0]	0	These bits contain the peak value determined in the current channel.
24	IPPHASE[0]	0	When this bit is set to 1, Phase A current generated IPEAKVAL[23:0] value.
25	IPPHASE[1]	0	When this bit is set to 1, Phase B current generated IPEAKVAL[23:0] value.
26	IPPHASE[2]	0	When this bit is set to 1, Phase C current generated IPEAKVAL[23:0] value.
31:27		00000	These bits are always 0.

Table 35. VPEAK Register (Address 0xE501)

Bit Location	Bit Mnemonic	Default Value	Description
23:0	VPEAKVAL[23:0]	0	These bits contain the peak value determined in the voltage channel.
24	VPPHASE[0]	0	When this bit is set to 1, Phase A voltage generated VPEAKVAL[23:0] value.
25	VPPHASE[1]	0	When this bit is set to 1, Phase B voltage generated VPEAKVAL[23:0] value.
26	VPPHASE[2]	0	When this bit is set to 1, Phase C voltage generated VPEAKVAL[23:0] value.
31:27		00000	These bits are always 0.

Table 36. STATUS0 Register (Address 0xE502)

Bit Location	Bit Mnemonic	Default Value	Description
0	AEHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the total active energy registers (AWATTHR, BWATTHR, or CWATTHR) has changed.
1	FAEHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the fundamental active energy registers, FWATTHR, BFWATTHR, or CFWATTHR, has changed.
2	REHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the total reactive energy registers (AVARHR, BVARHR, or CVARHR) has changed.
3	FREHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the fundamental reactive energy registers, AFVARHR, BFVARHR, or CFVARHR, has changed.
4	VAEHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the apparent energy registers (AVAHR, BVAHR, or CVAHR) has changed.
5	LENERGY	0	When this bit is set to 1, in line energy accumulation mode, it indicates the end of an integration over an integer number of half line cycles set in the LINECYC register.
6	REVAPA	0	When this bit is set to 1, it indicates that the Phase A active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 0 (AWSIGN) of the PHSIGN register (see Table 45).
7	REVAPB	0	When this bit is set to 1, it indicates that the Phase B active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 1 (BWSIGN) of the PHSIGN register (see Table 45).
8	REVAPC	0	When this bit is set to 1, it indicates that the Phase C active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 2 (CWSIGN) of the PHSIGN register (see Table 45).

Bit Location	Bit Mnemonic	Default Value	Description
9	REVPSUM1	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF1 datapath has changed sign. The sign itself is indicated in Bit 3 (SUM1SIGN) of the PHSIGN register (see Table 45).
10	REVRPA	0	When this bit is set to 1, it indicates that the Phase A reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 4 (AVARSIGN) of the PHSIGN register (see Table 45).
11	REVRPB	0	When this bit is set to 1, it indicates that the Phase B reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 5 (BVARSIGN) of the PHSIGN register (see Table 45).
12	REVRPC	0	When this bit is set to 1, it indicates that the Phase C reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 6 (CVARSIGN) of the PHSIGN register (see Table 45).
13	REVPSUM2	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF2 datapath has changed sign. The sign itself is indicated in Bit 7 (SUM2SIGN) of the PHSIGN register (see Table 45).
14	CF1		When this bit is set to 1, it indicates a high to low transition has occurred at CF1 pin; that is, an active low pulse has been generated. The bit is set even if the CF1 output is disabled by setting Bit 9 (CF1DIS) to 1 in the CFMODE register. The type of power used at the CF1 pin is determined by Bits[2:0] (CF1SEL[2:0]) in the CFMODE register (see Table 43).
15	CF2		When this bit is set to 1, it indicates a high-to-low transition has occurred at the CF2 pin; that is, an active low pulse has been generated. The bit is set even if the CF2 output is disabled by setting Bit 10 (CF2DIS) to 1 in the CFMODE register. The type of power used at the CF2 pin is determined by Bits[5:3] (CF2SEL[2:0]) in the CFMODE register (see Table 43).
16	CF3		When this bit is set to 1, it indicates a high-to-low transition has occurred at CF3 pin; that is, an active low pulse has been generated. The bit is set even if the CF3 output is disabled by setting Bit 11 (CF3DIS) to 1 in the CFMODE register. The type of power used at the CF3 pin is determined by Bits[8:6] (CF3SEL[2:0]) in the CFMODE register (see Table 43).
17	DREADY	0	When this bit is set to 1, it indicates that all periodical (at 8 kHz rate) DSP computations have finished.
18	REVPSUM3	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF3 datapath has changed sign. The sign itself is indicated in Bit 8 (SUM3SIGN) of the PHSIGN register (see Table 45).
31:19	Reserved	0 0000 0000 0000	Reserved. These bits are always 0.

Table 37. STATUS1 Register (Address 0xE503)

Bit Location	Bit Mnemonic	Default Value	Description
0	NLOAD	0	When this bit is set to 1, it indicates that at least one phase entered no load condition based on total active and reactive powers. The phase is indicated in Bits[2:0] (NLPHASE[x]) in the PHNOLOAD register (see Table 41).
1	FNLOAD	0	When this bit is set to 1, it indicates that at least one phase entered no load condition based on fundamental active and reactive powers. The phase is indicated in Bits[5:3] (FNLPHASE[x]) in PHNOLOAD register (see Table 41 in which this register is described).
2	VANLOAD	0	When this bit is set to 1, it indicates that at least one phase entered no load condition based on apparent power. The phase is indicated in Bits[8:6] (VANLPHASE[x]) in the PHNOLOAD register (see Table 41).
3	ZXTOVA	0	When this bit is set to 1, it indicates a zero crossing on Phase A voltage is missing.
4	ZXTOVB	0	When this bit is set to 1, it indicates a zero crossing on Phase B voltage is missing.
5	ZXTOVC	0	When this bit is set to 1, it indicates a zero crossing on Phase C voltage is missing.
6	ZXTOIA	0	When this bit is set to 1, it indicates a zero crossing on Phase A current is missing.
7	ZXTOIB	0	When this bit is set to 1, it indicates a zero crossing on Phase B current is missing.
8	ZXTOIC	0	When this bit is set to 1, it indicates a zero crossing on Phase C current is missing.
9	ZXVA	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase A voltage.
10	ZXVB	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase B voltage.
11	ZXVC	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase C voltage.
12	ZXIA	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase A current.

Bit Location	Bit Mnemonic	Default Value	Description
13	ZXIB	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase B current.
14	ZXIC	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase C current.
15	RSTDONE	1	In case of a software reset command, Bit 7 (SWRST) is set to 1 in the CONFIG register, or a hardware reset, this bit is set to 1 at the end of the transition process and after all registers changed value to default. The $\overline{\text{IRQ1}}$ pin goes low to signal this moment because this interrupt cannot be disabled.
16	SAG	0	When this bit is set to 1, it indicates a SAG event has occurred on one of the phases indicated by Bits[14:12] (VSPHASE[x]) in the PHSTATUS register (see Table 40).
17	OI	0	When this bit is set to 1, it indicates an overcurrent event has occurred on one of the phases indicated by Bits[5:3] (OIPHASE[x]) in the PHSTATUS register (see Table 40).
18	OV	0	When this bit is set to 1, it indicates an overvoltage event has occurred on one of the phases indicated by Bits[11:9] (OVPHASE[x]) in the PHSTATUS register (see Table 40).
19	SEQERR	0	When this bit is set to 1, it indicates a negative-to-positive zero crossing on Phase A voltage was not followed by a negative-to-positive zero crossing on Phase B voltage but by a negative-to-positive zero crossing on Phase C voltage.
20	MISMTCH	0	When this bit is set to 1, it indicates $\left\|\|ISUM\| - \|INWV\|\right\| > ISUMLVL$, where *ISUMLVL* is indicated in the ISUMLVL register.
21	Reserved	1	Reserved. This bit is always set to 1.
22	Reserved	0	Reserved. This bit is always set to 0.
23	PKI	0	When this bit is set to 1, it indicates that the period used to detect the peak value in the current channel has ended. The IPEAK register contains the peak value and the phase where the peak has been detected (see Table 34).
24	PKV	0	When this bit is set to 1, it indicates that the period used to detect the peak value in the voltage channel has ended. VPEAK register contains the peak value and the phase where the peak has been detected (see Table 35).
25	CRC	0	When this bit is set to 1, it indicates the ADE7978 has computed a different checksum relative to the one computed when the Run register was set to 1.
31:26	Reserved	000 0000	Reserved. These bits are always 0.

Table 38. MASK0 Register (Address 0xE50A)

Bit Location	Bit Mnemonic	Default Value	Description
0	AEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the total active energy registers (AWATTHR, BWATTHR, or CWATTHR) changes.
1	FAEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the fundamental active energy registers (AFWATTHR, BFWATTHR, or CFWATTHR) changes.
2	REHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the total reactive energy registers (AVARHR, BVARHR, CVARHR) changes.
3	FREHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the fundamental reactive energy registers (AFVARHR, BFVARHR, or CFVARHR) changes.
4	VAEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the apparent energy registers (AVAHR, BVAHR, or CVAHR) changes.
5	LENERGY	0	When this bit is set to 1, in line energy accumulation mode, it enables an interrupt at the end of an integration over an integer number of half line cycles set in the LINECYC register.
6	REVAPA	0	When this bit is set to 1, it enables an interrupt when the Phase A active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) changes sign.
7	REVAPB	0	When this bit is set to 1, it enables an interrupt when the Phase B active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) changes sign.
8	REVAPC	0	When this bit is set to 1, it enables an interrupt when the Phase C active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) changes sign.
9	REVPSUM1	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF1 datapath changes sign.
10	REVRPA	0	When this bit is set to 1, it enables an interrupt when the Phase A reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total or fundamental) changes sign.

Bit Location	Bit Mnemonic	Default Value	Description
11	REVRPB	0	When this bit is set to 1, it enables an interrupt when the Phase B reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total or fundamental) changes sign.
12	REVRPC	0	When this bit is set to 1, it enables an interrupt when the Phase C reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total or fundamental) changes sign.
13	REVPSUM2	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF2 datapath changes sign.
14	CF1		When this bit is set to 1, it enables an interrupt when a high-to-low transition occurs at the CF1 pin, that is, an active low pulse is generated. The interrupt can be enabled even if the CF1 output is disabled by setting Bit 9 (CF1DIS) to 1 in the CFMODE register. The type of power used at the CF1 pin is determined by Bits[2:0] (CF1SEL[2:0]) in the CFMODE register (see Table 43).
15	CF2		When this bit is set to 1, it enables an interrupt when a high-to-low transition occurs at CF2 pin, that is, an active low pulse is generated. The interrupt may be enabled even if the CF2 output is disabled by setting Bit 10 (CF2DIS) to 1 in the CFMODE register. The type of power used at the CF2 pin is determined by Bits[5:3] (CF2SEL[2:0]) in the CFMODE register (see Table 43).
16	CF3		When this bit is set to 1, it enables an interrupt when a high to low transition occurs at CF3 pin, that is, an active low pulse is generated. The interrupt may be enabled even if the CF3 output is disabled by setting Bit 11 (CF3DIS) to 1 in the CFMODE register. The type of power used at the CF3 pin is determined by Bits[8:6] (CF3SEL[2:0]) in the CFMODE register (see Table 43).
17	DREADY	0	When this bit is set to 1, it enables an interrupt when all periodical (at 8 kHz rate) DSP computations finish.
18	REVPSUM3	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF3 datapath changes sign.
31:19	Reserved	00 0000 0000 0000	Reserved. These bits do not manage any functionality.

Table 39. MASK1 Register (Address 0xE50B)

Bit Location	Bit Mnemonic	Default Value	Description
0	NLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters no load condition based on total active and reactive powers.
1	FNLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters no load condition based on fundamental active and reactive powers.
2	VANLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters no load condition based on apparent power.
3	ZXTOVA	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase A voltage is missing.
4	ZXTOVB	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase B voltage is missing.
5	ZXTOVC	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase C voltage is missing.
6	ZXTOIA	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase A current is missing.
7	ZXTOIB	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase B current is missing.
8	ZXTOIC	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase C current is missing.
9	ZXVA	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase A voltage.
10	ZXVB	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase B voltage.
11	ZXVC	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase C voltage.
12	ZXIA	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase A current.
13	ZXIB	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase B current.

Bit Location	Bit Mnemonic	Default Value	Description
14	ZXIC	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase C current.
15	RSTDONE	0	Because the RSTDONE interrupt cannot be disabled, this bit does not have any functionality attached. It can be set to 1 or cleared to 0 without having any effect.
16	SAG	0	When this bit is set to 1, it enables an interrupt when a SAG event occurs on one of the phases indicated by Bits[14:12] (VSPHASE[x]) in the PHSTATUS register (see Table 40).
17	OI	0	When this bit is set to 1, it enables an interrupt when an overcurrent event occurs on one of the phases indicated by Bits[5:3] (OIPHASE[x]) in the PHSTATUS register (see Table 40).
18	OV	0	When this bit is set to 1, it enables an interrupt when an overvoltage event occurs on one of the phases indicated by Bits[11:9] (OVPHASE[x]) in the PHSTATUS register (see Table 40).
19	SEQERR	0	When this bit is set to 1, it enables an interrupt when a negative-to-positive zero crossing on Phase A voltage is not followed by a negative-to-positive zero crossing on Phase B voltage, but by a negative-to-positive zero crossing on Phase C voltage.
20	MISMTCH	0	When this bit is set to 1, it enables an interrupt when $\left\|\|ISUM\| - \|INWV\|\right\| > ISUMLVL$ is greater than the value indicated in ISUMLVL register.
22:21	Reserved	00	Reserved. These bits do not manage any functionality.
23	PKI	0	When this bit is set to 1, it enables an interrupt when the period used to detect the peak value in the current channel has ended.
24	PKV	0	When this bit is set to 1, it enables an interrupt when the period used to detect the peak value in the voltage channel has ended.
25	CRC	0	When this bit is set to 1, it enables an interrupt when the latest checksum value is different from the checksum value computed when Run register was set to 1.
31:26	Reserved	000 0000	Reserved. These bits do not manage any functionality.

Table 40. PHSTATUS Register (Address 0xE600)

Bit Location	Bit Mnemonic	Default Value	Description
2:0	Reserved	000	Reserved. These bits are always 0.
3	OIPHASE[0]	0	When this bit is set to 1, Phase A current generates Bit 17 (OI) in the STATUS1 register.
4	OIPHASE[1]	0	When this bit is set to 1, Phase B current generates Bit 17 (OI) in the STATUS1 register.
5	OIPHASE[2]	0	When this bit is set to 1, Phase C current generates Bit 17 (OI) in the STATUS1 register.
8:6	Reserved	000	Reserved. These bits are always 0.
9	OVPHASE[0]	0	When this bit is set to 1, Phase A voltage generates Bit 18 (OV) in the STATUS1 register.
10	OVPHASE[1]	0	When this bit is set to 1, Phase B voltage generates Bit 18 (OV) in the STATUS1 register.
11	OVPHASE[2]	0	When this bit is set to 1, Phase C voltage generates Bit 18 (OV) in the STATUS1 register.
12	VSPHASE[0]	0	When this bit is set to 1, Phase A voltage generates Bit 16 (SAG) in the STATUS1 register.
13	VSPHASE[1]	0	When this bit is set to 1, Phase B voltage generates Bit 16 (SAG) in the STATUS1 register.
14	VSPHASE[2]	0	When this bit is set to 1, Phase C voltage generates Bit16 (SAG) in the STATUS1 register.
15	Reserved	0	Reserved. This bit is always 0.

Table 41. PHNOLOAD Register (Address 0xE608)

Bit Location	Bit Mnemonic	Default Value	Description
0	NLPHASE[0]	0	0: Phase A is out of no load condition based on total active/reactive powers. 1: Phase A is in no load condition based on total active/reactive powers. Bit set together with Bit 0 (NLOAD) in the STATUS1 register.
1	NLPHASE[1]	0	0: Phase B is out of no load condition based on total active/reactive powers. 1: Phase B is in no load condition based on total active/reactive powers. Bit set together with Bit 0 (NLOAD) in the STATUS1 register.
2	NLPHASE[2]	0	0: Phase C is out of no load condition based on total active/reactive powers. 1: Phase C is in no load condition based on total active/reactive powers. Bit set together with Bit 0 (NLOAD) in the STATUS1 register.
3	FNLPHASE[0]	0	0: Phase A is out of no load condition based on fundamental active/reactive powers. 1: Phase A is in no load condition based on fundamental active/reactive powers. This bit is

Bit Location	Bit Mnemonic	Default Value	Description
			set together with Bit 1 (FNLOAD) in STATUS1.
4	FNLPHASE[1]	0	0: Phase B is out of no load condition based on fundamental active/reactive powers. 1: Phase B is in no load condition based on fundamental active/reactive powers. This bit is set together with Bit 1 (FNLOAD) in STATUS1.
5	FNLPHASE[2]	0	0: Phase C is out of no load condition based on fundamental active/reactive powers. 1: Phase C is in no load condition based on fundamental active/reactive powers. This bit is set together with Bit 1 (FNLOAD) in STATUS1.
6	VANLPHASE[0]	0	0: Phase A is out of no load condition based on apparent power. 1: Phase A is in no load condition based on apparent power. Bit set together with Bit 2 (VANLOAD) in the STATUS1 register.
7	VANLPHASE[1]	0	0: Phase B is out of no load condition based on apparent power. 1: Phase B is in no load condition based on apparent power. Bit set together with Bit 2 (VANLOAD) in the STATUS1 register.
8	VANLPHASE[2]	0	0: Phase C is out of no load condition based on apparent power. 1: Phase C is in no load condition based on apparent power. Bit set together with Bit 2 (VANLOAD) in the STATUS1 register.
15:9	Reserved	000 0000	Reserved. These bits are always 0.

Table 42. COMPMODE Register (Address 0xE60E)

Bit Location	Bit Mnemonic	Default Value	Description
0	TERMSEL1[0]	1	Setting all TERMSEL1[2:0] to 1 signifies the sum of all three phases is included in the CF1 output. Phase A is included in the CF1 outputs calculations.
1	TERMSEL1[1]	1	Phase B is included in the CF1 outputs calculations.
2	TERMSEL1[2]	1	Phase C is included in the CF1 outputs calculations.
3	TERMSEL2[0]	1	Setting all TERMSEL2[2:0] to 1 signifies the sum of all three phases is included in the CF2 output. Phase A is included in the CF2 outputs calculations.
4	TERMSEL2[1]	1	Phase B is included in the CF2 outputs calculations.
5	TERMSEL2[2]	1	Phase C is included in the CF2 outputs calculations.
6	TERMSEL3[0]	1	Setting all TERMSEL3[2:0] to 1 signifies the sum of all three phases is included in the CF3 output. Phase A is included in the CF3 outputs calculations.
7	TERMSEL3[1]	1	Phase B is included in the CF3 outputs calculations.
8	TERMSEL3[2]	1	Phase C is included in the CF3 outputs calculations.
10:9	ANGLESEL[1:0]	00	00: the angles between phase voltages and phase currents are measured. 01: the angles between phase voltages are measured. 10: the angles between phase currents are measured. 11: no angles are measured.
11	VNOMAEN	0	When this bit is 0, the apparent power on Phase A is computed regularly. When this bit is 1, the apparent power on Phase A is computed using VNOM register instead of regular measured rms phase voltage.
12	VNOMBEN	0	When this bit is 0, the apparent power on Phase B is computed regularly. When this bit is 1, the apparent power on Phase B is computed using VNOM register instead of regular measured rms phase voltage.
13	VNOMCEN	0	When this bit is 0, the apparent power on Phase C is computed regularly. When this bit is 1, the apparent power on Phase C is computed using VNOM register instead of regular measured rms phase voltage.
14	SELFREQ	0	When the ADE7978 is connected to 50 Hz networks, this bit should be cleared to 0 (default value). When the ADE7978 is connected to 60 Hz networks, this bit should be set to 1.
15	Reserved	0	This bit is 0 by default and it does not manage any functionality.

Table 43. CFMODE Register (Address 0xE610)

Bit Location	Bit Mnemonic	Default Value	Description
2:0	CF1SEL[2:0]	000	000: the CF1 frequency is proportional to the sum of total active powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register.

Bit Location	Bit Mnemonic	Default Value	Description
			001: the CF1 frequency is proportional to the sum of total reactive powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 010: the CF1 frequency is proportional to the sum of apparent powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 011: the CF1 frequency is proportional to the sum of fundamental active powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 100: the CF1 frequency is proportional to the sum of fundamental reactive powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 101, 110, 111: reserved. When set, the CF1 signal is not generated.
5:3	CF2SEL[2:0]	001	000: the CF2 frequency is proportional to the sum of total active powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 001: the CF2 frequency is proportional to the sum of total reactive powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 010: the CF2 frequency is proportional to the sum of apparent powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 011: the CF2 frequency is proportional to the sum of fundamental active powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 100: the CF2 frequency is proportional to the sum of fundamental reactive powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 101,110,111: reserved. When set, the CF2 signal is not generated.
8:6	CF3SEL[2:0]	010	000: the CF3 frequency is proportional to the sum of total active powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 001: the CF3 frequency is proportional to the sum of total reactive powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 010: the CF3 frequency is proportional to the sum of apparent powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 011: CF3 frequency is proportional to the sum of fundamental active powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 100: CF3 frequency is proportional to the sum of fundamental reactive powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 101,110,111: reserved. When set, the CF3 signal is not generated.
9	CF1DIS	1	When this bit is set to 1, the CF1 output is disabled. The respective digital to frequency converter remains enabled even if CF1DIS = 1. When this bit is set to 0, the CF1 output is enabled.
10	CF2DIS	1	When this bit is set to 1, the CF2 output is disabled. The respective digital to frequency converter remains enabled even if CF2DIS = 1. When this bit is set to 0, the CF2 output is enabled.
11	CF3DIS	1	When this bit is set to 1, the CF3 output is disabled. The respective digital to frequency converter remains enabled even if CF3DIS = 1. When this bit is set to 0, the CF3 output is enabled.
12	CF1LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF1 pulse is generated. See the Synchronizing Energy Registers with CFx Outputs section.
13	CF2LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF2 pulse is generated. See the Synchronizing Energy Registers with CFx Outputs section.
14	CF3LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF3 pulse is generated. See the Synchronizing Energy Registers with CFx Outputs section.
15	Reserved	0	Reserved. This bit does not manage any functionality.

Table 44. APHCAL, BPHCAL, CPHCAL Registers (Address 0xE614, Address 0xE615, Address 0xE616)

Bit Location	Bit Mnemonic	Default Value	Description
9:0	PHCALVAL	0000000000	If current channel compensation is necessary, these bits can vary only between 0 and 383. If voltage channel compensation is necessary, these bits can vary only between 512 and 895. If the PHCALVAL bits are set with numbers between 384 and 511, the compensation behaves like PHCALVAL set between 0 and 127.

Bit Location	Bit Mnemonic	Default Value	Description
			If the PHCALVAL bits are set with numbers between 896 and 1023, the compensation behaves like PHCALVAL bits set between 512 and 639.
15:10	Reserved	000000	Reserved. These bits do not manage any functionality.

Table 45. PHSIGN Register (Address 0xE617)

Bit Location	Bit Mnemonic	Default Value	Description
0	AWSIGN	0	0: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase A is positive. 1: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase A is negative.
1	BWSIGN	0	0: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase B is positive. 1: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase B is negative.
2	CWSIGN	0	0: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase C is positive. 1: if the active power identified by Bit 6 (REVAPSEL) bit in the ACCMODE register (total of fundamental) on Phase C is negative.
3	SUM1SIGN	0	0: if the sum of all phase powers in the CF1 datapath is positive. 1: if the sum of all phase powers in the CF1 datapath is negative. Phase powers in the CF1 datapath are identified by Bits[2:0] (TERMSEL1[x]) of the COMPMODE register and by Bits[2:0] (CF1SEL[x]) of the CFMODE register.
4	AVARSIGN	0	0: if the reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total of fundamental) on Phase A is positive. 1: if the reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total of fundamental) on Phase A is negative.
5	BVARSIGN	0	0: if the reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total of fundamental) on Phase B is positive. 1: if the reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total of fundamental) on Phase B is negative.
6	CVARSIGN	0	0: if the reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total of fundamental) on Phase C is positive. 1: if the reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total of fundamental) on Phase C is negative.
7	SUM2SIGN	0	0: if the sum of all phase powers in the CF2 datapath is positive. 1: if the sum of all phase powers in the CF2 datapath is negative. Phase powers in the CF2 datapath are identified by Bits[5:3] (TERMSEL2[x]) of the COMPMODE register and by Bits[5:3] (CF2SEL[x]) of the CFMODE register.
8	SUM3SIGN	0	0: if the sum of all phase powers in the CF3 datapath is positive. 1: if the sum of all phase powers in the CF3 datapath is negative. Phase powers in the CF3 datapath are identified by Bits[8:6] (TERMSEL3[x]) of the COMPMODE register and by Bits[8:6] (CF3SEL[x]) of the CFMODE register.
15:9	Reserved	000 0000	Reserved. These bits are always 0.

Table 46. CONFIG Register (Address 0xE618)

Bit Location	Bit Mnemonic	Default Value	Description
1:0	ZX_DREADY	00	This bit manages the output signal at ZX/ $\overline{\text{DREADY}}$ pin: 00: $\overline{\text{DREADY}}$ functionality is enabled (see Digital Signal Processor section). 01: ZX functionality generated by phase A voltage (see Zero-Crossing Detection). 10: ZX functionality generated by phase B voltage (see Zero-Crossing Detection). 11: ZX functionality generated by phase C voltage (see Zero-Crossing Detection).
2	Reserved	0	Reserved. This bit is always 0.
3	SWAP	0	When this bit is set to 1, the voltage channel outputs VA, VB, VC and VN are swapped with the current channel outputs IA, IB, IC and IN, repectively. Thus, the current channel

Bit Location	Bit Mnemonic	Default Value	Description
			information is present in the phase voltage channel registers and vice versa.
4	HPFEN	1	When HPFEN = 1, then all high-pass filters in voltage and current channels are enabled. When HPFEN = 0, then all high-pass filters are disabled.
5	LPFSEL	0	When LPFSEL = 0, the LPF in the total active power data path introduces a settling time of 650 ms. When LPFSEL = 1, the LPF in the total active power data path introduces a settling time of 1300 ms.
6	HSDCEN	0	When this bit is set to 1, the HSDC serial port is enabled and HSCLK functionality is chosen at CF3/HSCLK pin. When this bit is cleared to 0, HSDC is disabled and CF3 functionality is chosen at CF3/HSCLK pin.
7	SWRST	0	When this bit is set to 1, a software reset is initiated.
9:8	VTOIA[1:0]	00	These bits decide what phase voltage is considered together with Phase A current in the power path. 00 = Phase A voltage. 01 = Phase B voltage. 10 = Phase C voltage. 11 = reserved. When set, the ADE7978 behaves like VTOIA[1:0] = 00.
11:10	VTOIB[1:0]	00	These bits decide what phase voltage is considered together with Phase B current in the power path. 00 = Phase B voltage. 01 = Phase C voltage. 10 = Phase A voltage. 11 = reserved. When set, the ADE7978 behaves like VTOIB[1:0] = 00.
13:12	VTOIC[1:0]	00	These bits decide what phase voltage is considered together with Phase C current in the power path. 00 = Phase C voltage. 01 = Phase A voltage. 10 = Phase B voltage. 11 = reserved. When set, the ADE78978 behaves like VTOIC[1:0] = 00.
14	INSEL	0	When INSEL = 0, the register NIRMS contains the rms value of the neutral current. When INSEL = 1, the register NIRMS contains the rms value of ISUM, the instantaneous value of the sum of all 3 phase currents, IA, IB, and IC.
15	Reserved	0	Reserved. This bit does not manage any functionality.

Table 47. MMODE Register (Address 0xE700)

Bit Location	Bit Mnemonic	Default Value	Description
1:0	Reserved	00	Reserved. These bits do not manage any functionality.
2	PEAKSEL[0]	1	PEAKSEL[2:0] bits can all be set to 1 simultaneously to allow peak detection on all three phases simultaneously. If more than one PEAKSEL[2:0] bits are set to 1, then the peak measurement period indicated in the PEAKCYC register decreases accordingly because zero crossings are detected on more than one phase. When this bit is set to 1, Phase A is selected for the voltage and current peak registers.
3	PEAKSEL[1]	1	When this bit is set to 1, Phase B is selected for the voltage and current peak registers.
4	PEAKSEL[2]	1	When this bit is set to 1, Phase C is selected for the voltage and current peak registers.
7:5	Reserved	000	Reserved. These bits do not manage any functionality.

Table 48. ACCMODE Register (Address 0xE701)

Bit Location	Bit Mnemonic	Default Value	Description
1:0	WATTACC[1:0]	00	00: signed accumulation mode of the total and fundamental active powers. The total and fundamental active energy registers and the CFx pulses are generated in the same way. 01: positive only accumulation mode of the total and fundamental active powers. In this mode, although the total and fundamental active energy registers are accumulated in positive only mode, the CFx pulses are generated in signed accumulation mode.

Bit Location	Bit Mnemonic	Default Value	Description
			10: reserved. When set, the device behaves like WATTACC[1:0] = 00. 11: absolute accumulation mode of the total and fundamental active powers. The total and fundamental energy registers and the CFx pulses are generated in the same way.
3:2	VARACC[1:0]	00	00: signed accumulation of total and fundamental reactive powers. The reactive energy registers and the CFx pulses are generated in the same way. 01: reserved. When set, the device behaves like VARACC[1:0] = 00. 10: the total and fundamental reactive powers are accumulated depending on the sign of, respectively, the total and fundamental active power: if the active power is positive, the reactive power is accumulated as is, whereas if the active power is negative, the reactive power is accumulated with reversed sign. The total and fundamental reactive energy registers and the CFx pulses are generated in the same way. 11: absolute accumulation mode of the total and fundamental reactive powers. In this mode, although the total and fundamental reactive energy registers are accumulated in absolute mode, the CFx pulses are generated in signed accumulation mode.
5:4	CONSEL[1:0]	00	These bits select the inputs to the energy accumulation registers. IA′, IB′, and IC′ are IA, IB, and IC shifted respectively by −90°. See Table 49. 00: 3-phase four wires with three voltage sensors. 01: 3-phase three wires delta connection. 10: 3-phase four wires with two voltage sensors. 11: 3-phase four wires delta connection.
6	REVAPSEL	0	0: The total active power on each phase is used to trigger a bit in the STATUS0 register as follows: on Phase A triggers Bit 6 (REVAPA), on Phase B triggers Bit 7 (REVAPB), and on Phase C triggers Bit 8 (REVAPC). 1: The fundamental active power on each phase is used to trigger a bit in the STATUS0 register as follows: on Phase A triggers Bit 6 (REVAPA), on Phase B triggers Bit 7 (REVAPB), and on Phase C triggers Bit 8 (REVAPC).
7	REVRPSEL	0	0: The total reactive power on each phase is used to trigger a bit in the STATUS0 register as follows: on Phase A triggers Bit 10 (REVRPA), on Phase B triggers Bit 11 (REVRPB), and on Phase C triggers Bit 12 (REVRPC). 1: The fundamental reactive power on each phase is used to trigger a bit in the STATUS0 register as follows: on Phase A triggers Bit 10 (REVRPA), on Phase B triggers Bit 11 (REVRPB), and on Phase C triggers Bit 12 (REVRPC).

Table 49. CONSEL[1:0] Bits in Energy Registers[1]

Energy Registers	CONSEL[1:0] = 00	CONSEL[1:0] = 01	CONSEL[1:0] = 10	CONSEL[1:0] = 11
AWATTHR, AFWATTHR	VA × IA	VA × IA	VA × IA	VA × IA
BWATTHR, BFWATTHR	VB × IB	VB = VA – VC	VB = –VA – VC	VB = –VA
		VB ×IB[1]	VB × IB	VB × IB
CWATTHR, CFWATTHR	VC × IC	VC × IC	VC × IC	VC × IC
AVARHR, AFVARHR	VA × IA′	VA × IA′	VA × IA′	VA × IA′
BVARHR, BFVARHR	VB × IB′	VB = VA – VC	VB = –VA – VC	VB = –VA
		VB × IB ′[1]	VB × IB′	VB × IB′
CVARHR, CFVARHR	VC ×IC′	VC × IC′	VC × IC′	VC × IC′
AVAHR	VA rms × IA rms	VA rms × IA rms	VA rms × IA rms	VA rms × IA rms
BVAHR	VB rms × IB rms	VB rms × IB rms[1]	VB rms × IB rms	VB rms × IB rms
		VB = VA – VC	VB=-VA-VC	VB=-VA
CVAHR	VC rms × IC rms	VC rms × IC rms	VC rms × IC rms	VC rms × IC rms

[1] In a 3-phase three wire case (CONSEL[1:0] = 01), the ADE7978 computes the rms value of the line voltage between Phase A and and Phase C and stores the result into BVRMS register (see the Voltage RMS in 3-Phase Three Wire Delta Configurations section). The Phase B current determined after the HPF is 0. Consequently, the powers associated with Phase B are 0. To avoid any errors in the frequency output pins (CF1, CF2, or CF3) related to the powers associated with Phase B, disable the contribution of Phase B to the energy-to-frequency converters by setting bits TEMSEL1[1] or TERMSEL2[1] or TERMSEL3[1] to 0 in the COMPMODE register (see the Energy-to-Frequency Conversion section).

Table 50. LCYCMODE Register (Address 0xE702)

Bit Location	Bit Mnemonic	Default Value	Description
0	LWATT	0	0: the watt-hour accumulation registers (AWATTHR, BWATTHR, CWATTHR, AFWATTHR,

Bit Location	Bit Mnemonic	Default Value	Description
			BFWATTHR, and CFWATTHR) are placed in regular accumulation mode. 1: the watt-hour accumulation registers (AWATTHR, BWATTHR, CWATTHR, AFWATTHR, BFWATTHR, and CFWATTHR) are placed into line cycle accumulation mode.
1	LVAR	0	0: the var-hour accumulation registers (AVARHR, BVARHR, and CVARHR) are placed in regular accumulation mode. 1: the var-hour accumulation registers (AVARHR, BVARHR, and CVARHR) are placed into line-cycle accumulation mode.
2	LVA	0	0: the VA-hour accumulation registers (AVAHR, BVAHR, and CVAHR) are placed in regular accumulation mode. 1: the VA-hour accumulation registers (AVAHR, BVAHR, and CVAHR) are placed into line-cycle accumulation mode.
3	ZXSEL[0]	1	0: Phase A is not selected for zero-crossings counts in the line cycle accumulation mode. 1: Phase A is selected for zero-crossings counts in the line cycle accumulation mode. If more than one phase is selected for zero-crossing detection, the accumulation time is shortened accordingly.
4	ZXSEL[1]	1	0: Phase B is not selected for zero-crossings counts in the line cycle accumulation mode. 1: Phase B is selected for zero-crossings counts in the line cycle accumulation mode.
5	ZXSEL[2]	1	0: Phase C is not selected for zero-crossings counts in the line cycle accumulation mode. 1: Phase C is selected for zero-crossings counts in the line cycle accumulation mode.
6	RSTREAD	1	0: read-with-reset of all energy registers is disabled. Clear this bit to 0 when Bits[2:0] (LWATT, LVAR, and LVA) are set to 1. 1: enables read-with-reset of all xWATTHR, xVARHR, xVAHR, xFWATTHR, and xFVARHR registers. This means a read of those registers resets them to 0.
7	PFMODE	0	0: power factor calculation uses instantaneous values of various phase powers used in its expression. 1: power factor calculation uses phase energies values calculated using line cycle accumulation mode. Bits LWATT and LVA in LCYCMODE register must be enabled for the power factors to be computed correctly. The update rate of the power factor measurement in this case is the integral number of half line cycles that are programmed into the LINECYC register.

Table 51. HSDC_CFG Register (Address 0xE706)

Bit Location	Bit Mnemonic	Default Value	Description
0	HCLK	0	0: HSCLK is 8 MHz. 1: HSCLK is 4 MHz.
1	HSIZE	0	0: HSDC transmits the 32-bit registers in 32-bit packages, most significant bit first. 1: HSDC transmits the 32-bit registers in 8-bit packages, most significant bit first.
2	HGAP	0	0: no gap is introduced between packages. 1: a gap of seven HCLK cycles is introduced between packages.
4:3	HXFER[1:0]	00	00 = HSDC transmits sixteen 32-bit words in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, INWV, AVA, BVA, CVA, AWATT, BWATT, CWATT, AVAR, BVAR, and CVAR. 01 = HSDC transmits seven instantaneous values of currents and voltages: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, and INWV. 10 = HSDC transmits nine instantaneous values of phase powers: AVA, BVA, CVA, AWATT, BWATT, CWATT, AVAR, BVAR, and CVAR. 11 = reserved. If set, the ADE7978 behave as if HXFER[1:0] = 00.
5	HSAPOL	0	0: $\overline{SS}$/HSA output pin is active low. 1: $\overline{SS}$/HSA output pin is active high.
7:6	Reserved	00	Reserved. These bits do not manage any functionality.

Table 52. CONFIG3 Register (Address 0xE708)

Bit Location	Bit Mnemonic	Default Value	Description

0	VA2_EN	1	Selects V2P or temperature measurement on Phase A ADE7933/ADE7932. If VA2_EN is set to 1, the default value, the V2P input is sensed on the second voltage channel of the ADE7933/ADE7932. If VA2_ENis cleared to 0, the temperature sensor is measured on the second voltage channel of the ADE7933/ADE7932.
1	VB2_EN	1	Selects V2P or temperature measurement on Phase B ADE7933/ADE7932. If VB2_EN is set to 1, the default value, the V2P input is sensed on the second voltage channel of the ADE7933/ADE7932. If VB2_ENis cleared to 0, the temperature sensor is measured on the second voltage channel of the ADE7933/ADE7932.
2	VC2_EN	1	Selects V2P or temperature measurement on Phase C ADE7933/ADE7932. If VC2_EN is set to 1, the default value, the V2P input is sensed on the second voltage channel of the ADE7933/ADE7932. If VC2_ENis cleared to 0, the temperature sensor is measured on the second voltage channel of the ADE7933/ADE7932.
3	VN2_EN	1	Selects V2P or temperature measurement on neutral line ADE7933/ADE7932. If VN2_EN is set to 1, the default value, the V2P input is sensed on the second voltage channel of the ADE7933/ADE7932. If VN2_ENis cleared to 0, the temperature sensor is measured on the second voltage channel of the ADE7933/ADE7932.
5,4	Reserved	00	Reserved. These bits do not manage any functionality.
6	CLKOUT_DIS	0	When this bit is set to 1, the ADE7933/ADE7932 CLKOUT pin is set high and no clock is generated.
7	ADE7933_SWRST	0	When this bit is set to 1, a software reset of the ADE7933/ADE7932s is initiated. See ADE7933/ADE7932 Software Reset Functionality section for details.

Table 53. CONFIG2 Register (Address 0xEA00)

Bit Location	Bit Mnemonic	Default Value	Description
0	I2C_LOCK	0	When this bit is 0, the $\overline{SS}$/HSA pin can be toggled three times to activate the SPI port. If I^2C is the active serial port, this bit must be set to 1 to lock it in. From this moment on, spurious toggling of the $\overline{SS}$/HSA pin and an eventual switch into using the SPI port is no longer possible. If SPI is the active serial port, any write to CONFIG register locks the port. From this moment on, a switch into using I^2C port is no longer possible. Once locked, the serial port choice is maintained when the ADE7978/ADE7933/ADE7932 chipset is software reset. A hardware reset unlocks the serial port selection and activates the I^2C, the default serial port.
7:1	Reserved	000000	Reserved. These bits do not manage any functionality.

OUTLINE DIMENSIONS

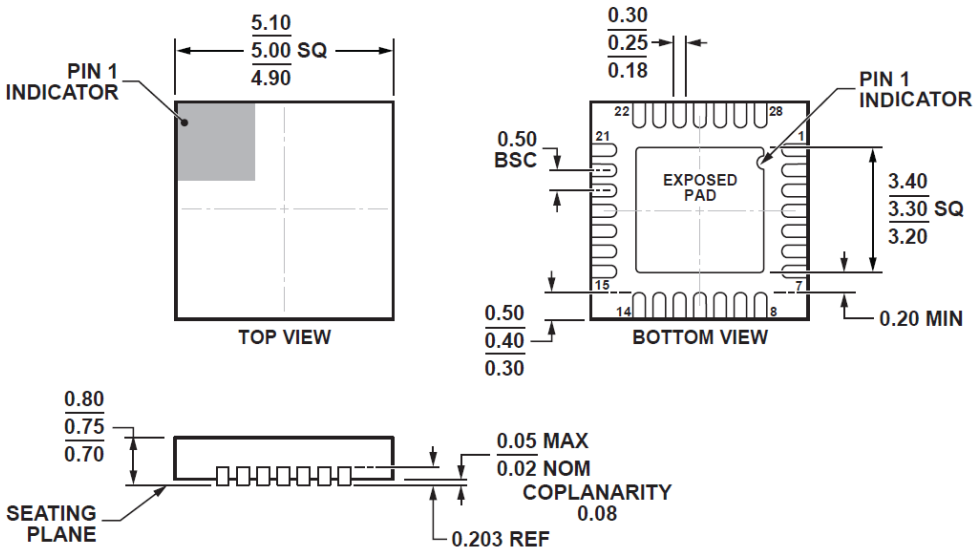


Figure 96. ADE7978 28-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5mm x 5 mm Body, Very Very Thin Quad, (CP-28-6)
Dimensions shown in millimeters

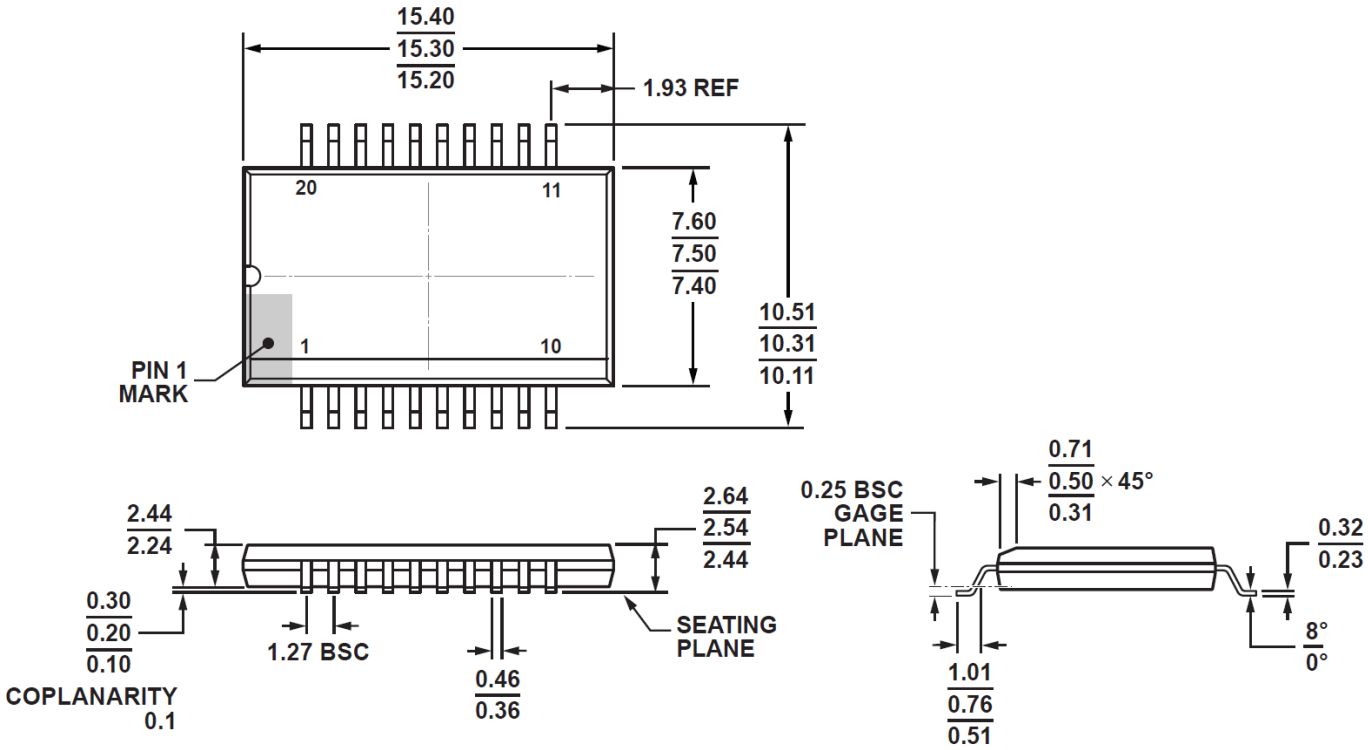


Figure 97. ADE7933/ADE7932 20-Lead Standard Small Outline Package, with increased Creepage [SOIC_IC]
Wide Body, (RI-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADE7978ACPZ	–40°C to +85°C	28-Lead LFCSP_WQ	CP-28-6
ADE7978ACPZ-RL	–40°C to +85°C	28-Lead LFCSP_WQ, 13″Tape and Reel	CP-28-6
ADE7933ARIZ	–40°C to +85°C	20-Lead SOIC_W	RI-20-1
ADE7933ARIZ-RL	–40°C to +85°C	20-Lead SOIC_W, 13″Tape and Reel	RI-20-1

Model[1]	Temperature Range	Package Description	Package Option
ADE7932ARIZ	–40°C to +85°C	20-Lead SOIC_W	RI-20-1
ADE7932ARIZ-RL	–40°C to +85°C	20-Lead SOIC_W, 13" Tape and Reel	RI-20-1
EVAL-ADE7978EBZ		Evaluation Board	
EVAL-SDP-CB1Z[2]		Evaluation System Controller Board	

[1] Z = RoHS Compliant Part.
[2] The EVAL-SDP-CB1Z is the controller board that manages the EVAL-ADE7978EBZ evaluation board. They need to be ordered together.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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